

Study of Single Event effects in electronic components

S.Blasko, G.Castellini, Y.H.Chang, E.Cortina, T.S.Dai, P.Emmonet,
L.Gallin-Martel, Ch.Haller, K.Hangarter, V.Hermel, A.Kounine,
V.Koutsenko, S.C.Lee, C.H.Lin, Y.K.Lin, M.Menichelli, A.Papi,
V.Plyaskine, Z.Ren, D.Shardt, R.Simon, M.Steuer, W.Wallraff

Abstract

Single Event Effects in electronic components are studied using heavy ion beams in the range of LET values from 5 to 60 MeV/(mg/cm²). Single Event Latchup and Upset rates are measured for several commercial-grade components. Projections to the ISS radiation environment are made.

1 Introduction

In space applications Single Event Effects in electronic components are found to be of comparable importance to the total radiation dose effects.

AMS Data Acquisition System will be based on commercial-grade electronic components. This note presents studies of those which we plan to use for building AMS DAQ. The studies are performed at GSI using Xe^{54} , Au^{79} and U^{92} beams of 100–800 MeV/nucl. Two effects are investigated: Single Event Upsets and Single Event Latchups

The measured SEE rates are used to estimate the behaviour of these components on board of ISS.

2 Experimental setup

The experimental layout is presented in Figure 1. Detailed description of the experimental setup is given in [1], in the present note only the most important features are mentioned. Fluxes of heavy ions are measured by the upstream Multi-wire Proportional Chamber and the downstream scintillator counter. MWPC is also used to monitor spatial distribution of ions in the plane transverse to the beam. Unit Under Test is monitored by the Control Logic box for SEE counts. Latchup protector controls current through UUT and switches power off in case of persistent overcurrent. DAQ PC collects information on fluences and SEE rates and stores it for further analysis.

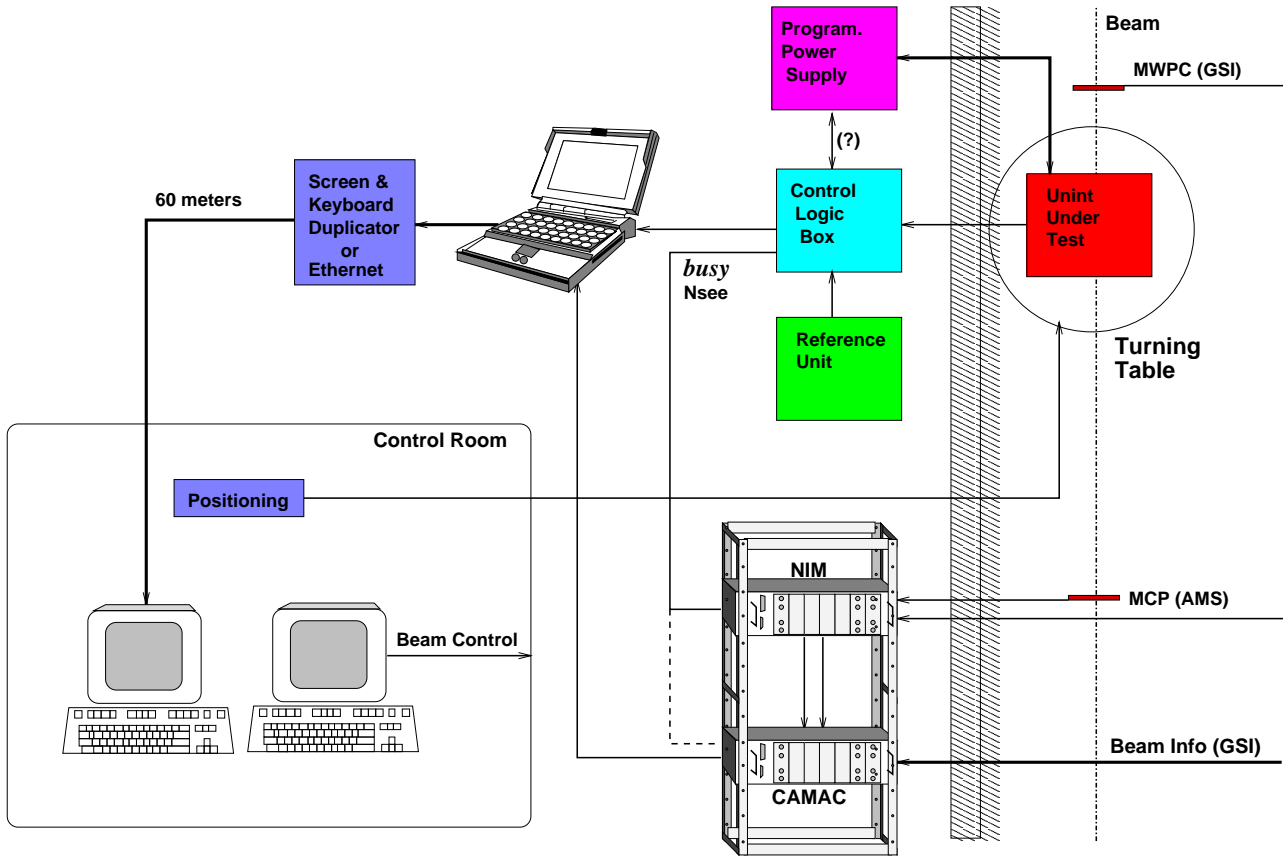


Figure 1: Beam test setup.

Unit Under Test is mounted on a motorised rotary stage with three inclination angles to the beam (0, 30 and 60 degree). The UUT positioning with respect to the beam line is done to an accuracy of 1 mm using a laser alignment system.

3 Heavy ion beams

Energy range for each beam is 100–800 MeV/nucl. Beam extraction time (i.e. spill duration) is chosen to be 5 sec and time between spills is in the range 4–6 sec. Intensities of $10^4 - 10^5$

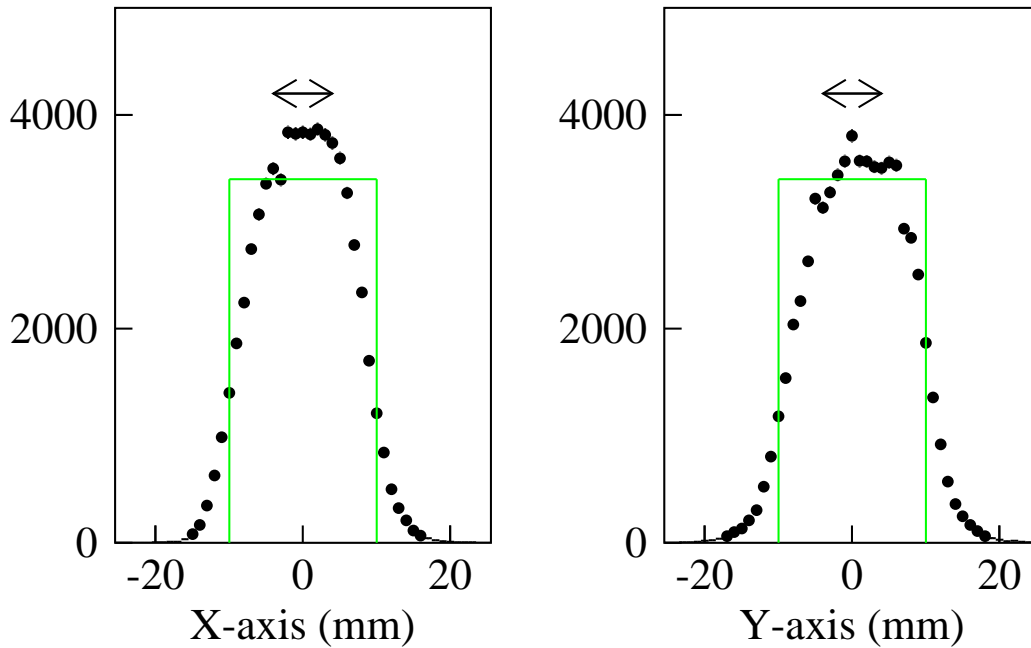
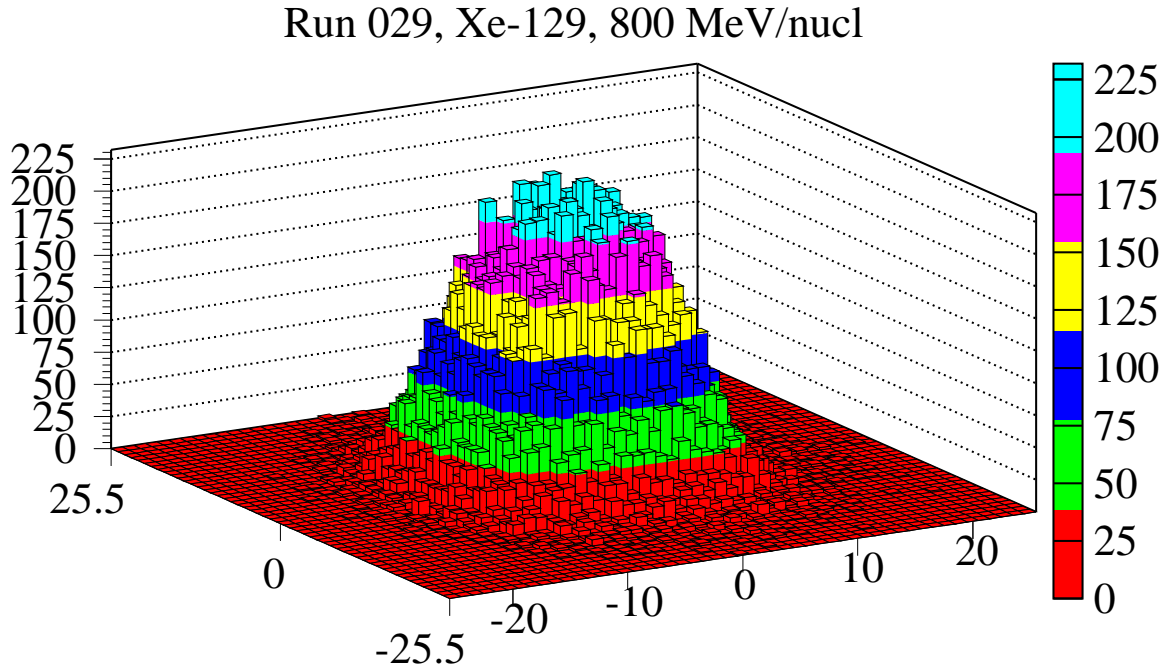


Figure 2: Typical beam shape. Component size is indicated by arrows.

ions/spill are used.

Beam spot on target has a Gaussian shape with a characteristic size (FWHM) of 5 mm. Even illumination of a larger area in the vicinity of a target is achieved by raster scan of a square area of $2 \cdot 2\text{cm}^2$. This technique provides high degree of spatial uniformity of the ion flux through the target which is positioned at the center of the scan area. The scan is not continuous, but from one pixel to another. Typically one complete scan corresponds to 90 pixels with 135 ions/pixel. Number of scans per spill depends on the beam intensity and ranges from 1 to 10. On a new spill scan continues from the pixel it stopped at the end of the previous spill.

One measurement (corresponding to an integral flux of $10^5 - 10^6 \frac{\text{ion}}{\text{cm}^2}$, one beam type and energy, and one incident angle) lasts 5-10 minutes and consists of about 40 spills.

4 Analysis procedures

LET values for each beam are calculated using the SRIM Monte Carlo program [2]. Chip packaging material is accounted for in the calculations. Figure 3 shows the effective LET along the path of 100 MeV/nucl Au^{79} ions. Uncertainty in the thickness of the plastic chip cover of 0.2 mm and uncertainty of the depth of the SEE sensitive layer in the silicon amount to about 5–15% of systematic uncertainty in the LET value at 100 MeV/nucl for all three ion beams. This uncertainty is negligible at 400 and 800 MeV/nucl.

The available ion energies cover the LET range from 5 to 45 MeV/(mg/cm²) (Table 1). The LET values in the table are calculated assuming the plastic cover thickness of 0.8 mm and silicon thickness of 0.2 mm.

Results for chip inclination angles of 30° and 60° are presented assuming $\text{LET}^*(\alpha) = \text{LET}(0)/\cos(\alpha)$. This assumption works well for one beam type and low SEU thresholds ($< 10 \text{ MeV}/(\text{mg}/\text{cm}^2)$) as demonstrated in Figure 4, where the normalised SEU cross sec-

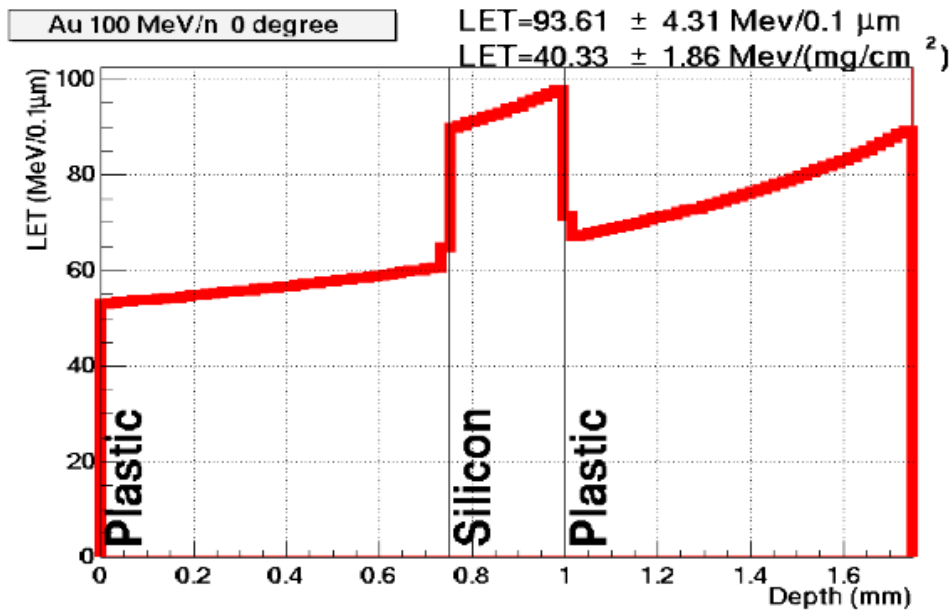


Figure 3: Effective LET value for 100 MeV/nucl Au^{79} ions as a function of the depth in a chip.

Table 1: LET values and ranges of GSI ion beams in Silicon

Beam energy (MeV/nucl)	100	200	400	800
Xe ⁵⁴ LET (Mev/mg/cm ²)	19.5	11.3	7.6	5.8
Xe ⁵⁴ RNG in Si (mm)	2.2	6.7	20.1	57.0
Au ⁷⁹ LET (Mev/mg/cm ²)	40.3	23.8	16.1	12.4
Au ⁷⁹ RNG in Si (mm) (mm)	1.7	4.9	14.4	40.0
U ⁹² LET (Mev/mg/cm ²)	58.8	32.0	21.8	16.8
U ⁹² RNG in Si (mm) (mm)	1.6	4.6	13.0	36.0

tion ($\sigma_{\text{SEU}}^k(\alpha)/\sigma_{\text{SEU}}^k(0)$) for all three beams ($k = \text{Xe}^{54}, \text{Au}^{79}$ and U^{92}) combined is shown as a function of the incidence angle α . However this is not a good approximation for cross sections corresponding to different beams but the same LET* value.

The uncertainty in the chip position of 1 mm in X and Y as well as the uncertainty in the dimensions of SEE sensitive surface (conservatively assumed to be 1 mm in both dimensions) are translated into the systematic error on the flux estimate of approximately 10%.

If the chip is not operational 100% of the time during the spill, special corrections must be

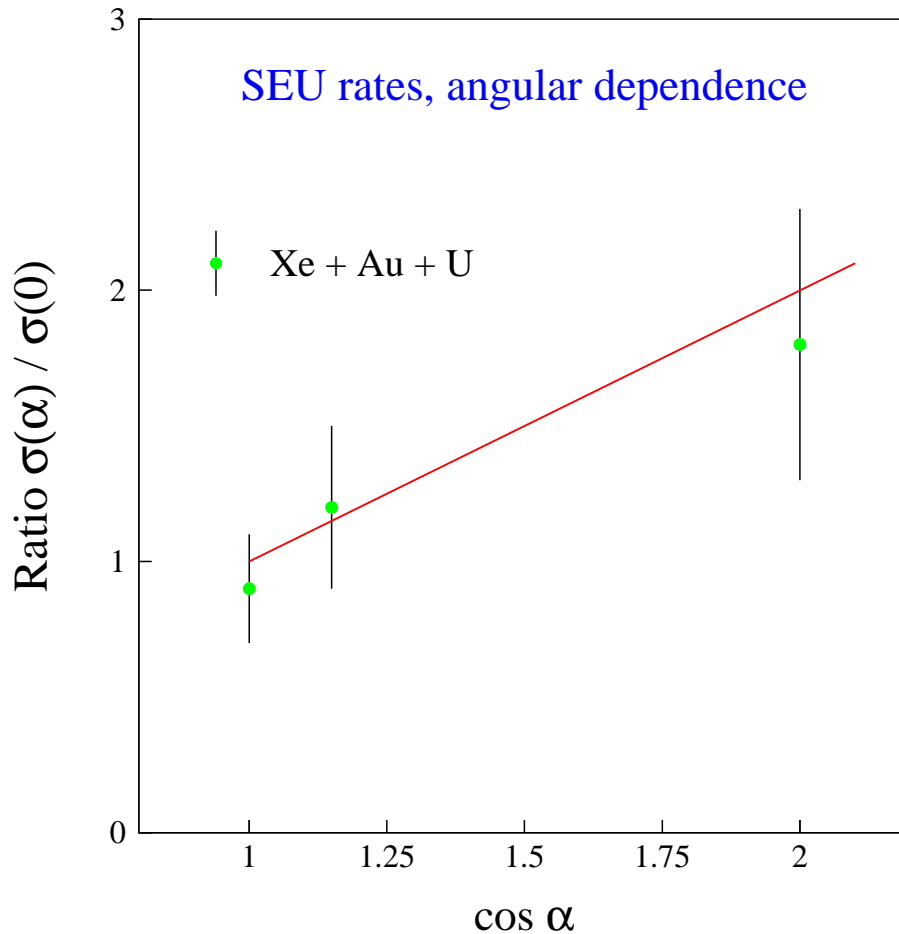


Figure 4: The angular dependence of SEU rates for the Watchdog timer.

applied to the flux estimates. The corrections depend on number of tests made before SEE is detected and on whether chip is actually irradiated during these tests. For bulk of the tested chips these corrections are small, but sometimes (for instance ADSP218x SEU and MHV100 SEU tests) they reach factor 2 or even more.

All other systematic uncertainties, which are not specifically identified, are estimated from the reproducibility of the measurements of the number of SEE in the very same conditions. A systematic error on N_{SEE} is estimated to be on the order of 20% using this approach.

Fluxes on ISS are calculated using the CREAM96 Monte Carlo program [3]. An example of simulated LET fluxes (summer 2003, ISS orbit, in absence of solar events) integrated over all ions with $Z = 2 - 92$ is presented in Figure 5. SEE rate in a component is expressed as follows:

$$R_{\text{SEE}}^{\text{ISS}} = \int_{\text{LET}} \Phi^{\text{ISS}}(\text{LET}) \cdot \sigma_{\text{SEE}}(\text{LET}) d(\text{LET}) \quad (1)$$

where $\sigma_{\text{SEE}}(\text{LET})$ is the measured SEE cross section. It follows from the shape of the spectrum presented in Figure 5 that components with high SEE threshold (above 10 MeV/(mg/cm²)) are not much sensitive to ISS fluxes independent on the cross-section value.

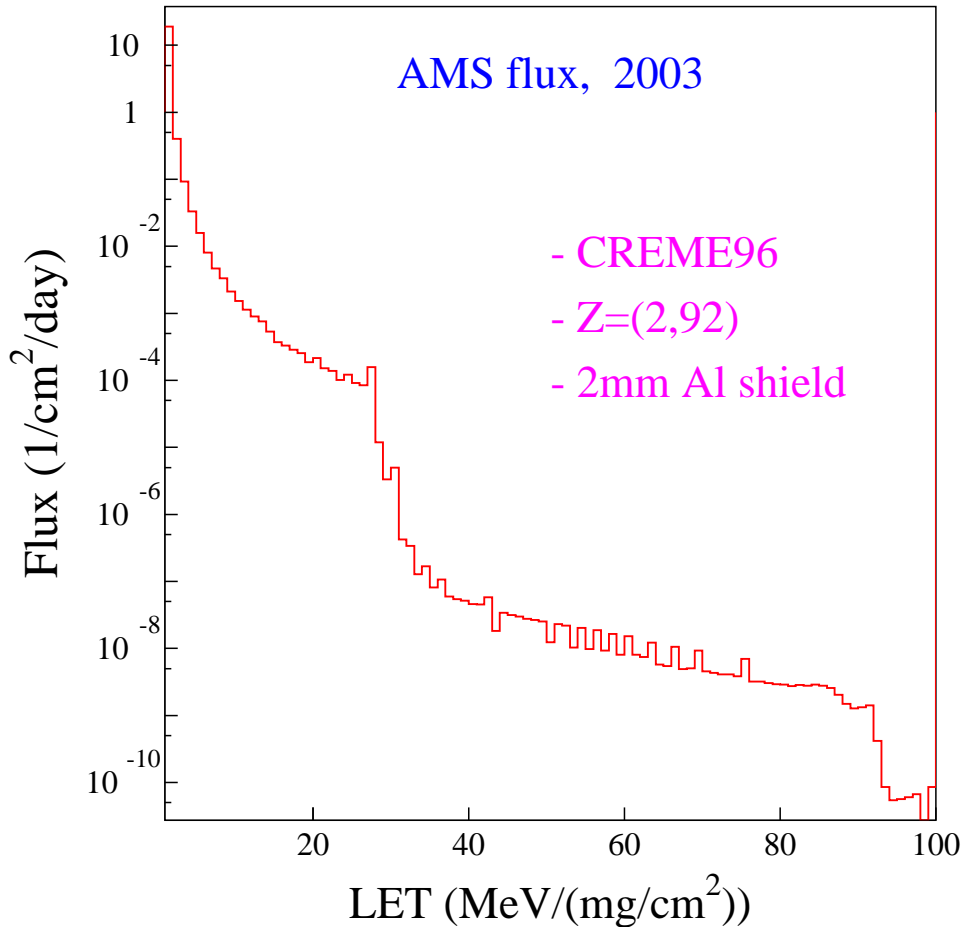


Figure 5: Expected fluxes on ISS in 2003.

5 ADSP2187L

Perugia SELDP board is used to detect overcurrent, to power off DSP and to generate a corresponding SEL signal. SELDP reaction time is estimated to be $1.2 \mu\text{s}$. DSP is powered on again at the end of that spill by the DAQ Computer.

Chip area of $4 \times 8\text{mm}^2$ is predominantly occupied by 160 KB of Program and Data Memory. A program that permanently runs in DSP checks the content of approximately 70% of the memory. If the program crashes, or memory error is detected, Control Logic Box generates a SEU signal and DAQ Computer cycles power on DSP at the end of the spill.

Fluences for the SEL and SEU cross section measurements are counted independently from the beginning of the spill until the corresponding SEE signal arrives. These fluences are corrected for the time when chip is not getting any ions due to the raster scan procedure.

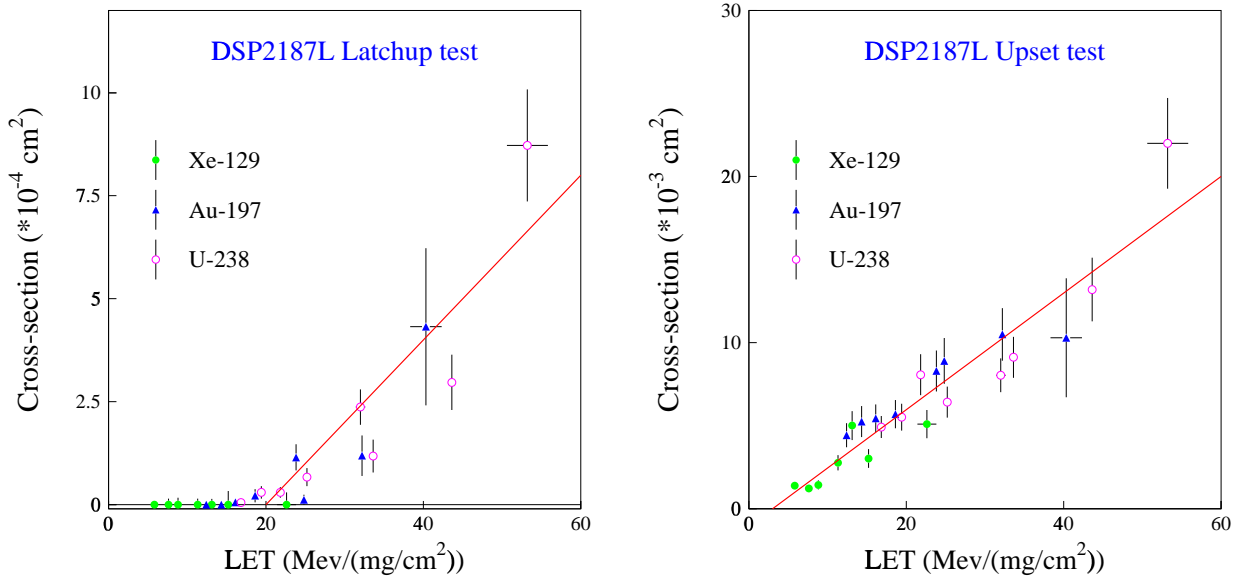


Figure 6: ADSP2187L – SEE rates as measured in GSI

The measured SEE cross sections are presented in Figure 6. Red lines correspond to the analytical function in Equation 1. Performing the integration, the SEE rates per day on ISS are estimated to be: $(8 \pm 3) \times 10^{-8}$ for SEL and $(10_{-4}^{+12}) \times 10^{-5}$ for SEU rates. The dominant uncertainty results from the accuracy of the threshold determination.

6 ADSP2189M

Perugia SELDP board is used to detect overcurrent, to power off DSP and to generate a corresponding SEL signal. SELDP reaction time is estimated to be $1.2 \mu\text{s}$. If powered off during the spill, DSP is powered on again at the end of that spill by the DAQ Computer.

Chip area of $4 \times 8\text{mm}^2$ is predominantly occupied by 192 KB of Program and Data Memory. A program that permanently runs in DSP checks the content of approximately 70% of the memory. If the program crashes, or memory error is detected, Control Logic Box generates a SEU signal and DAQ Computer stops counting SEU flux. However DSP stays powered on to continue measuring SEL cross section.

Fluences for the SEL and SEU cross section measurements are counted independently from the beginning of the spill until the corresponding SEE signal arrives. These fluences are corrected for the time when chip is not getting any ions due to the raster scan procedure.

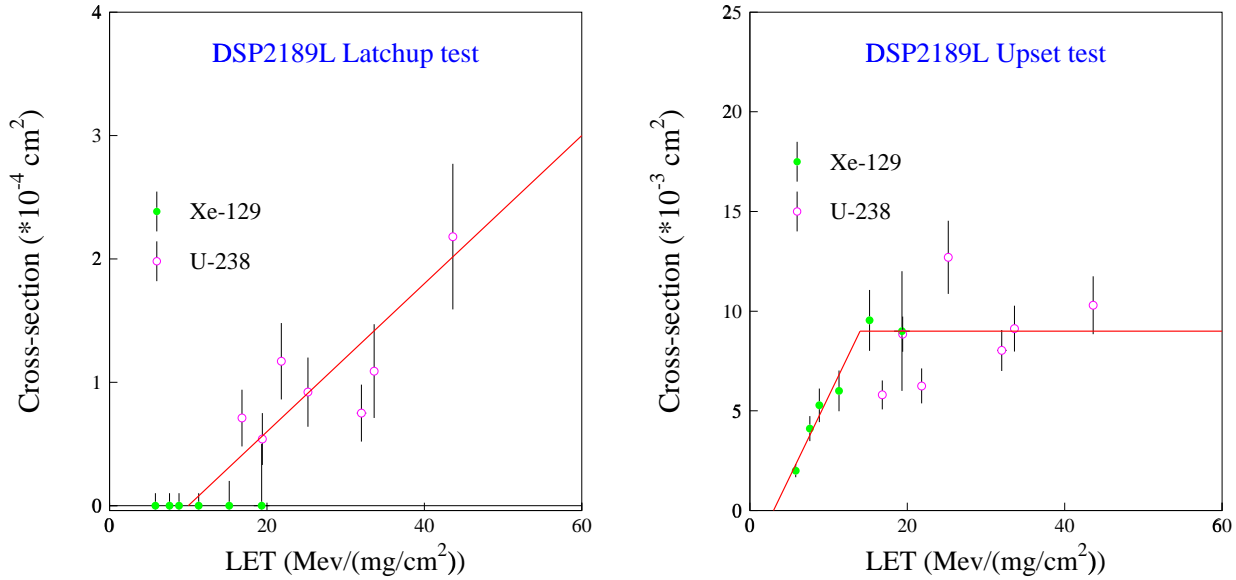


Figure 7: ADSP2189M – SEE rates as measured in GSI

The measured SEE cross sections are presented in Figure 7. Red lines correspond to the analytical function in Equation 1. Performing the integration, the SEE rates per day on ISS are estimated to be: 2×10^{-7} for SEL and $(2_{-1}^{+2}) \times 10^{-4}$ for SEU rates. The dominant uncertainty results from the accuracy of the threshold determination.

7 Tracker components

Perugia SELDP board is used to detect overcurrent, to power off UUT and to generate a corresponding SEL signal. SELDP reaction time is estimated to be $1.2 \mu\text{s}$. UUT is powered on again at the end of that spill by the DAQ Computer.

Detection of SEU is performed by comparing pattern of signals generated by UUT and Reference Unit in response to the same input sequence from CLB.

Since occurrence of SEU does not affect the functionality of any tracker component only one fluence for the SEL is measured from the beginning of the spill until the SEL signal arrives.

Flux corrections discussed in the previous sections are not yet implemented.

Results of HCC tests are presented in Figure 8. No upsets are observed for this component. The latchup threshold is found to be $17 \text{ MeV}/(\text{mg}/\text{cm}^2)$ and the SEL rate per day on ISS is estimated to be: 1.5×10^{-8} .

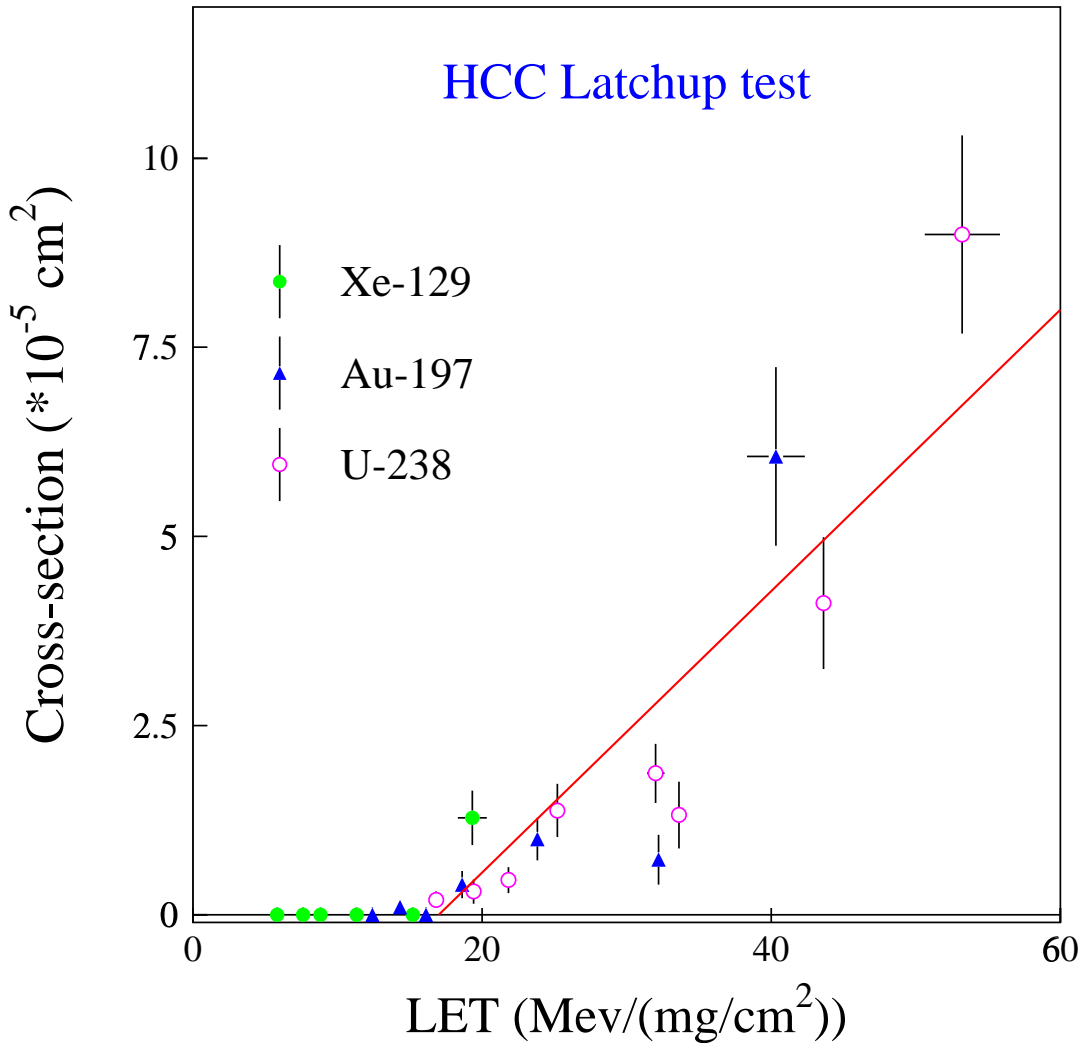


Figure 8: HCC – SEL rates as measured in GSI

Results of ISO150 tests are presented in Figure 9. No latchups are observed for this component. The SEU threshold is found to be low and outside the accessible LET range. Assuming that it is $1 \text{ MeV}/(\text{mg}/\text{cm}^2)$, the SEU rate per day on ISS is estimated to be 4.6×10^{-4} .

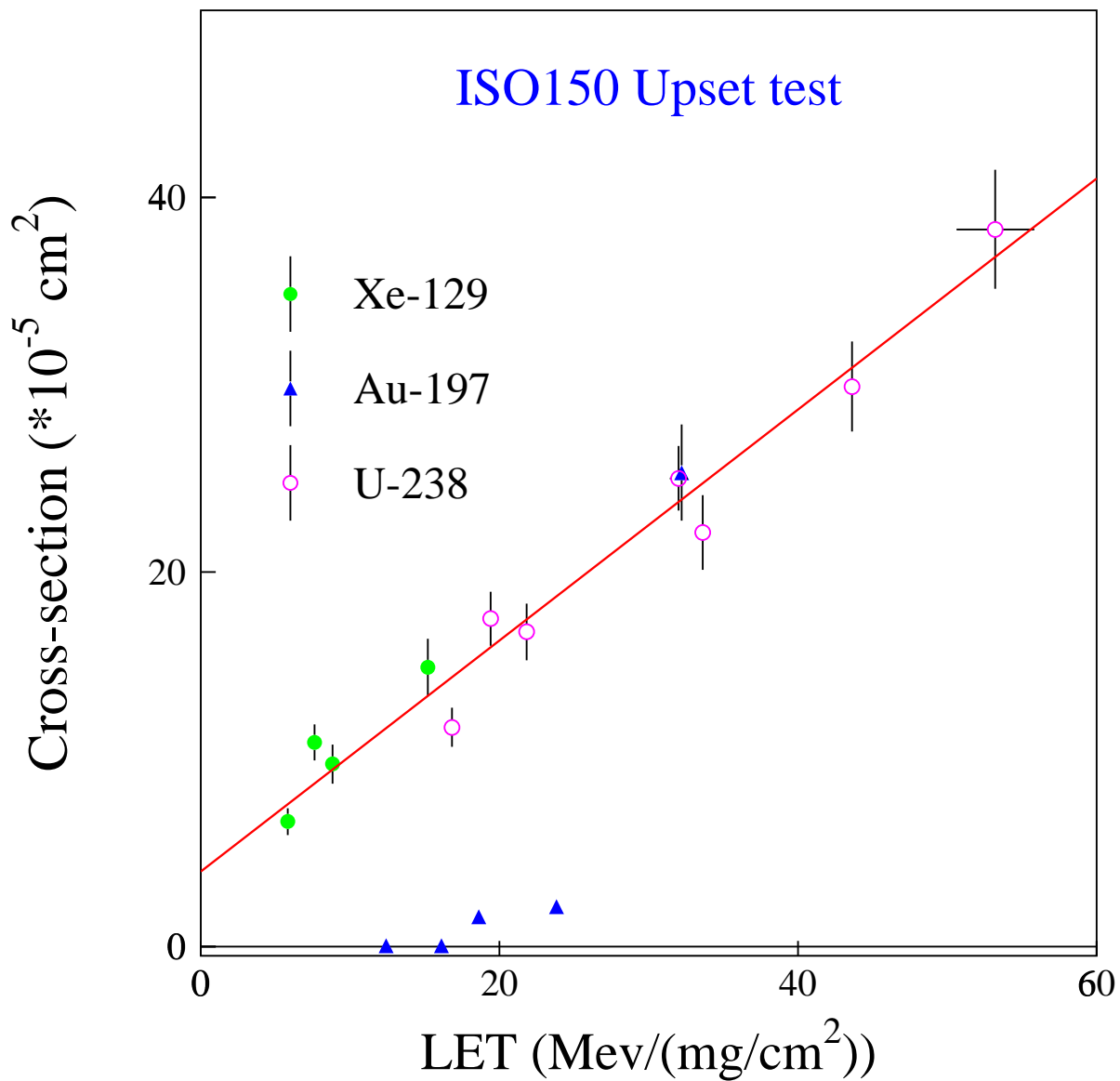


Figure 9: ISO150 – SEU rates as measured in GSI

Results of ADM tests are presented in Figure 10. No upsets are detected for this component. The latchup threshold is found to be 20 MeV/(mg/cm²) and the SEL rate per day on ISS is estimated to be: 6×10^{-9} .

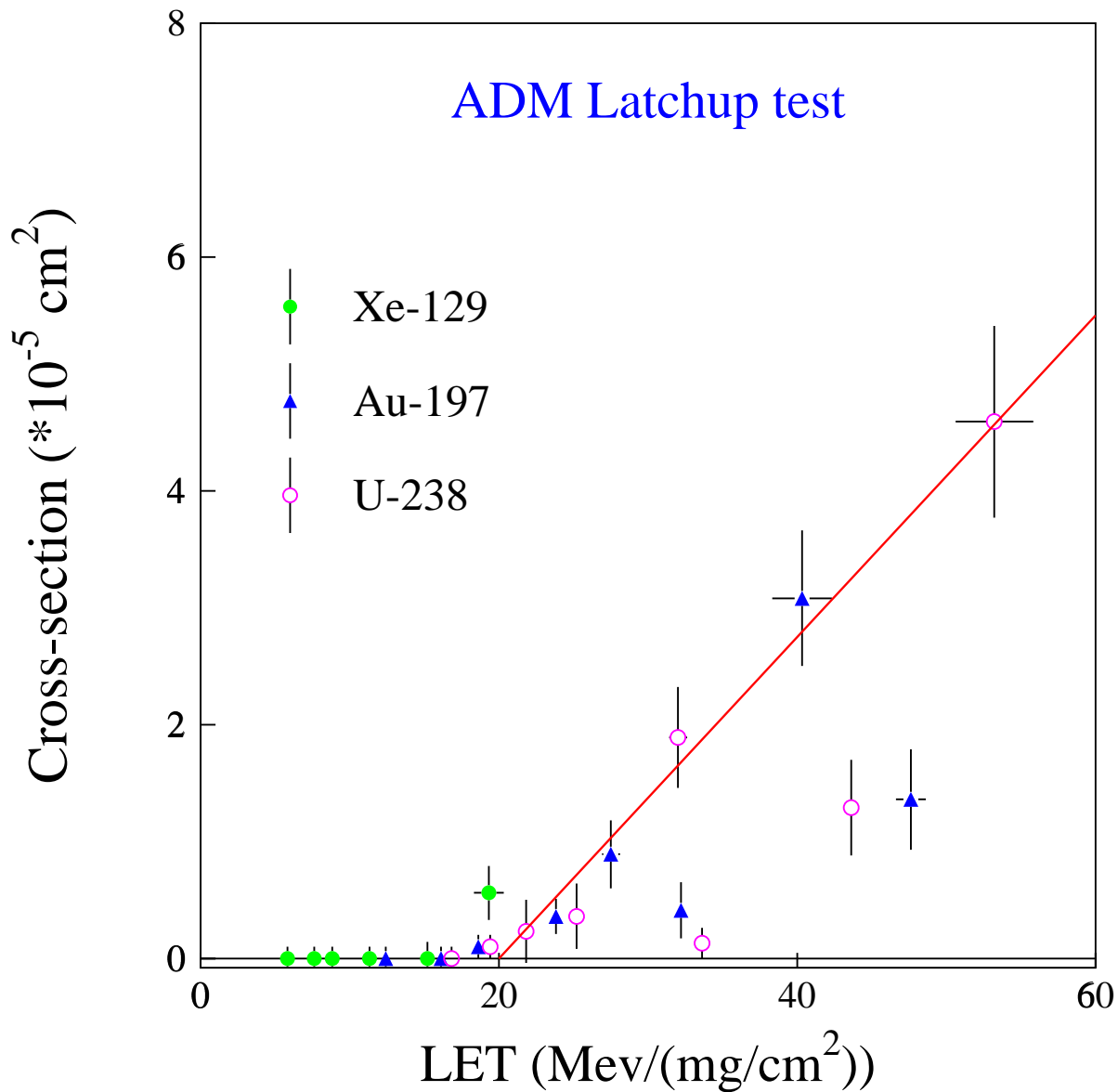


Figure 10: ADM – SEL rates as measured in GSI

Results of ADS803U tests are presented in Figure 11. The latchup threshold is found to be 20 MeV/(mg/cm²) and the SEL rate per day on ISS is estimated to be: 3×10^{-9} . The SEU threshold is found to be 22 MeV/(mg/cm²) and the SEL rate per day on ISS is estimated to be: 2×10^{-7} .

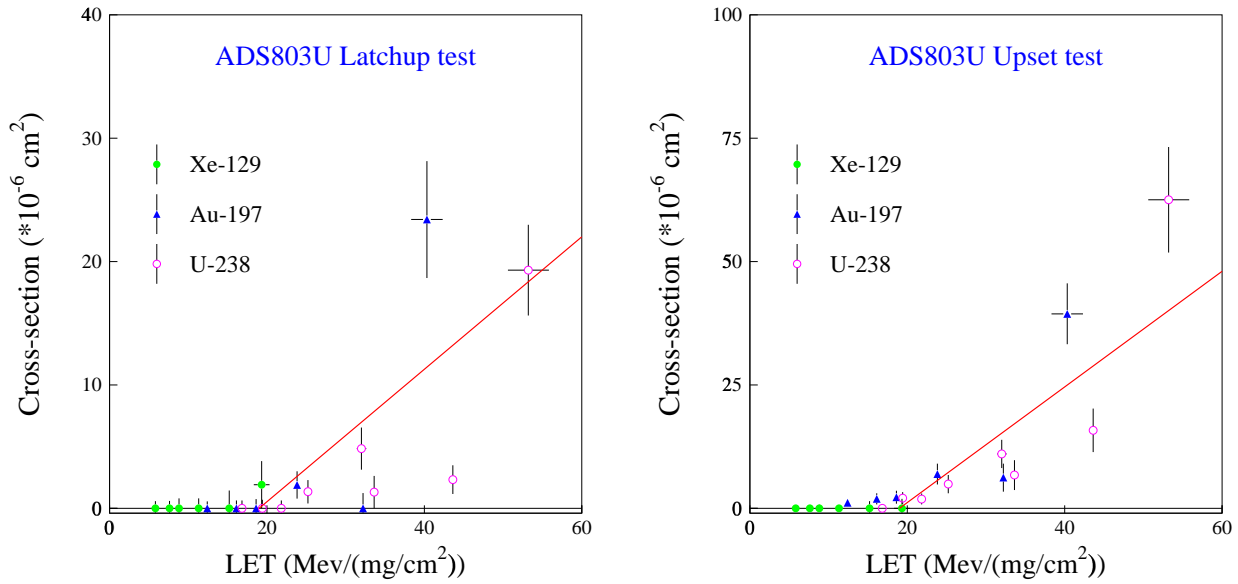


Figure 11: ADS803U – SEU rates as measured in GSI

Results of VA (old and new) tests are presented in Figure 12. The latchup threshold is found to be 10 MeV/(mg/cm²) for the old VA chip and 22 MeV/(mg/cm²) for the new one. The SEL rates per day on ISS is estimated to be: 1.2×10^{-6} and 1.6×10^{-8} for the old and new VA chips, respectively.

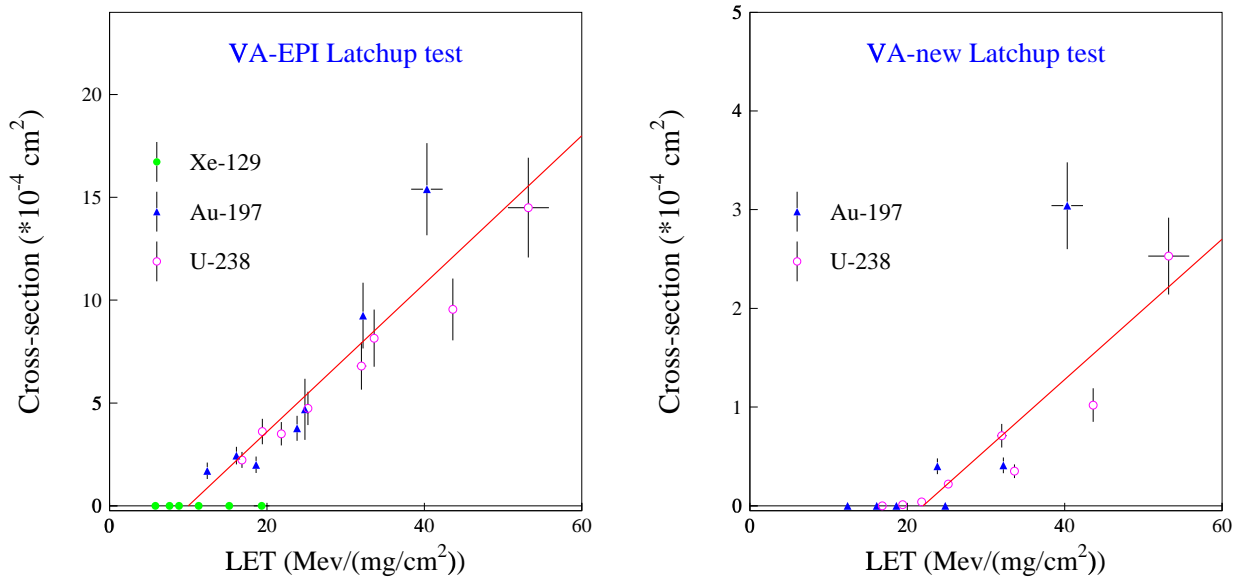


Figure 12: The new VA – SEL rates as measured in GSI

7.1 EMC FE chip

Only latchup tests were performed and only the analog part of this chip was tested. It amounts to approximately 0.06 mm^2 . No UUT functional tests were performed during the SEL measurements. Perugia SELDP board is used to detect overcurrent, to power off UUT and to generate a corresponding SEL signal. SELDP reaction time is estimated to be $1.2 \mu\text{s}$. UUT is powered on again at the end of that spill by the DAQ Computer.

No latchups were observed resulting in an upper limit on the SEL cross section of $2 \times 10^{-6} \text{ cm}^2$

7.2 RICH FE chip

Perugia SELDP board is used to detect overcurrent, to power off UUT and to generate a corresponding SEL signal. SELDP reaction time is estimated to be $1.2 \mu\text{s}$. UUT is powered on again at the end of that spill by the DAQ Computer.

SEU is detected as a digitised amplitude above threshold (no analog signal is present on input).

Flux calculation is corrected for the UUT power off time. Results are presented in Figure 13. SEL threshold is found to be approximately $18 \text{ MeV}/(\text{mg}/\text{cm}^2)$. SEU threshold is approximately $14 \text{ MeV}/(\text{mg}/\text{cm}^2)$.

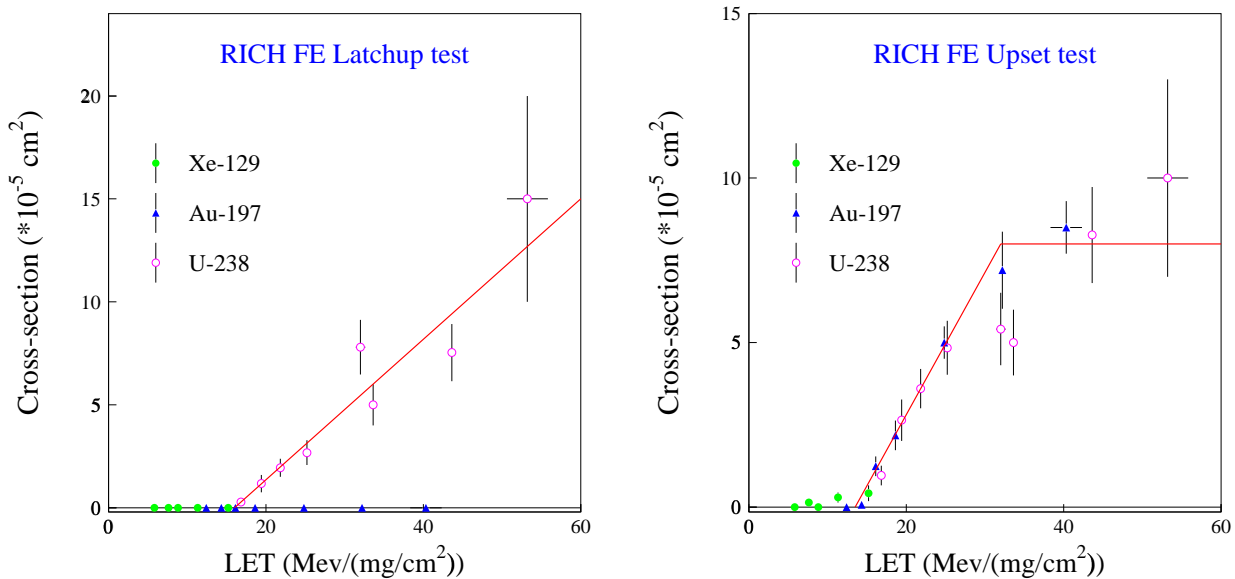


Figure 13: RICH front-end chip – SEE rates as measured in GSI

Two types of technologies were tested: AMS and DMILL. Results presented are for the AMS chip. The DMILL chip was tested using only U^{92} beam. No SELs were observed in the LET range $\sim 16 - 53 \text{ MeV}/(\text{mg}/\text{cm}^2)$. No SEU tests were performed for the DMILL chip.

The SEE rates per day on ISS are estimated to be: $(4 \pm 1) \times 10^{-8}$ for SEL and $(8 \pm 1) \times 10^{-8}$ for SEU.

8 Watchdog timer, AMD679

Watchdog timer has an on-board latchup protection. It is powered at the beginning of the measurement and switched off only at the end of the measurement. If latchup occurs the Control Logic Box powers off the UUT and generate a corresponding SEL signal. In that case UUT is powered on again at the end of that spill by the DAQ Computer.

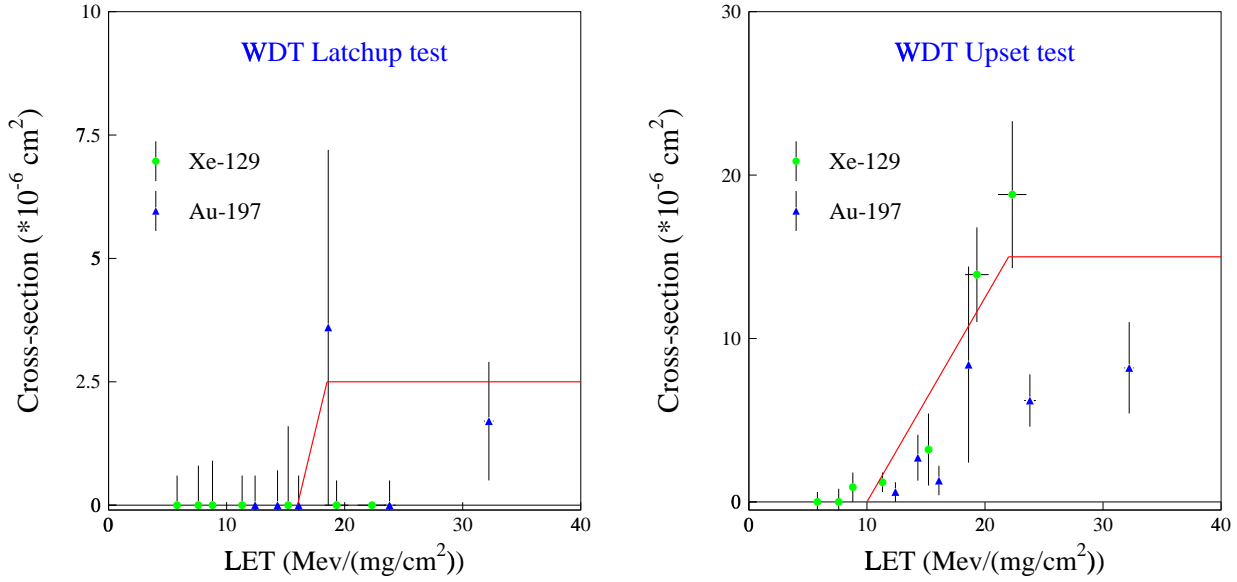


Figure 14: Watchdog timer – SEE rates as measured in GSI

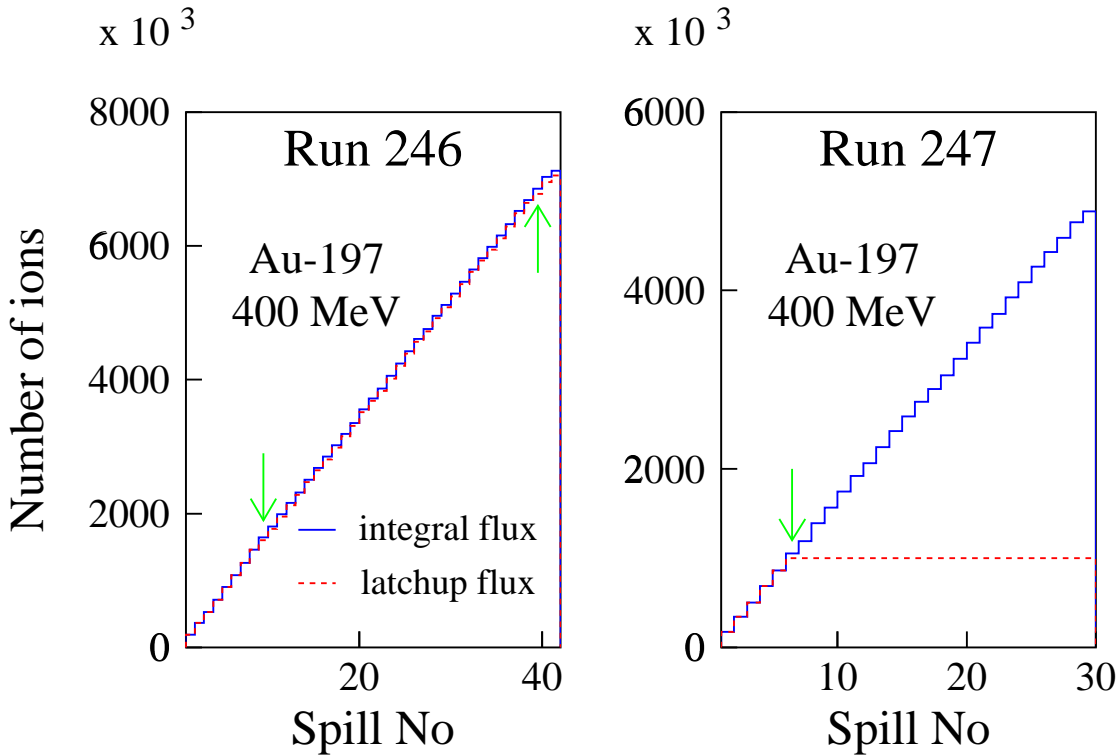


Figure 15: The integral flux (solid line) and the flux corrected for the DUT dead time (dashed line) for (a) Run 246 and (b) Run 247. Latchup occurrences are indicated by arrows.

Two types of SEU tests were performed: short tests and long tests. The “short” test (85 μs long) aims at detection of the “reset” signal generated by the Watchdog timer which would correspond to an upset. Under normal conditions this signal should not be generated. The long test (115 μs) - SEU is detected either as a presence of the “reset” signal in first 85 μs or as an absence of the “reset” signal after 100 μs . No statistically significant difference was observed between the SEU numbers for “short” and “long” tests with Xe^{54} beam. Only ‘short’ tests were performed with Au^{79} and U^{92} beams. Number of upsets is counted by the CLB during a spill and is reported on request to the DAQ PC between spills.

Flux calculation is corrected for the UUT power off time. Results are presented in Figure 14. SEL threshold is found to be approximately 16 $\text{MeV}/(\text{mg}/\text{cm}^2)$. SEU threshold is approximately 10 $\text{MeV}/(\text{mg}/\text{cm}^2)$. Starting from LET values 25 – 30 $\text{MeV}/(\text{mg}/\text{cm}^2)$ the measurements are not very reliable due to difficulties in initialising the chip. A likely explanation is that the latchup protection circuit was damaged in the run 247 (Au^{79} , 400 MeV/nucl). Starting from this run the first latchup that happens leads to persistent “power off” signal for the remainder of the run. This is illustrated in Figure 15, where the flux corrected for the dead time is compared with the total integral flux for the two runs exhibiting very different behaviour.

The SEE rates per day on ISS are estimated to be: $(5 \pm 1) \times 10^{-9}$ for SEL and $(4 \pm 1) \times 10^{-8}$ for SEU.

9 CPLD, CY37256P160

CPLD has an on-board latchup protection. It is powered at the beginning of the measurement and switched off only at the end of the measurement. If latchup occurs the Control Logic Box powers off the UUT and generate a corresponding SEL signal. In that case UUT is powered on again at the end of that spill by the DAQ Computer. The measured latchup cross section is presented in Figure 16.

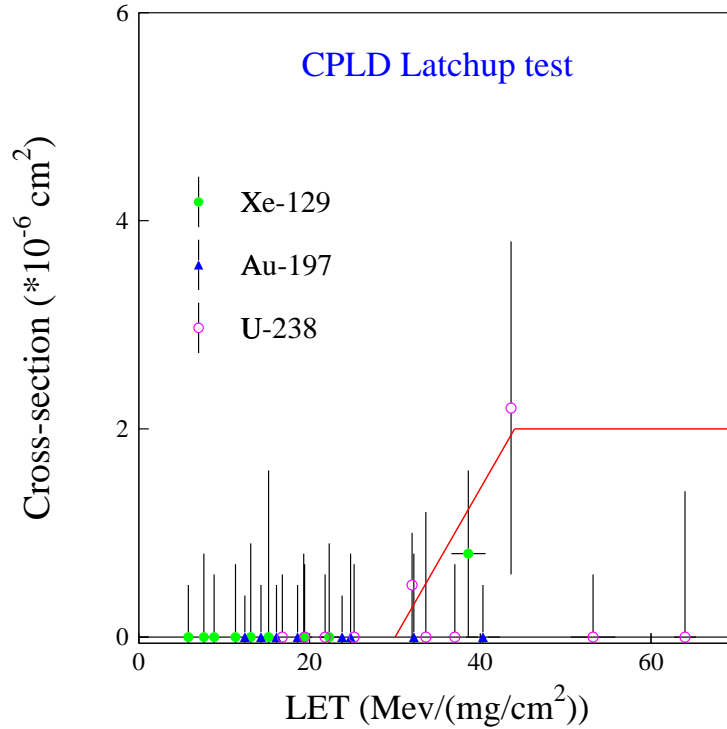


Figure 16: CPLD – SEL rates as measured in GSI

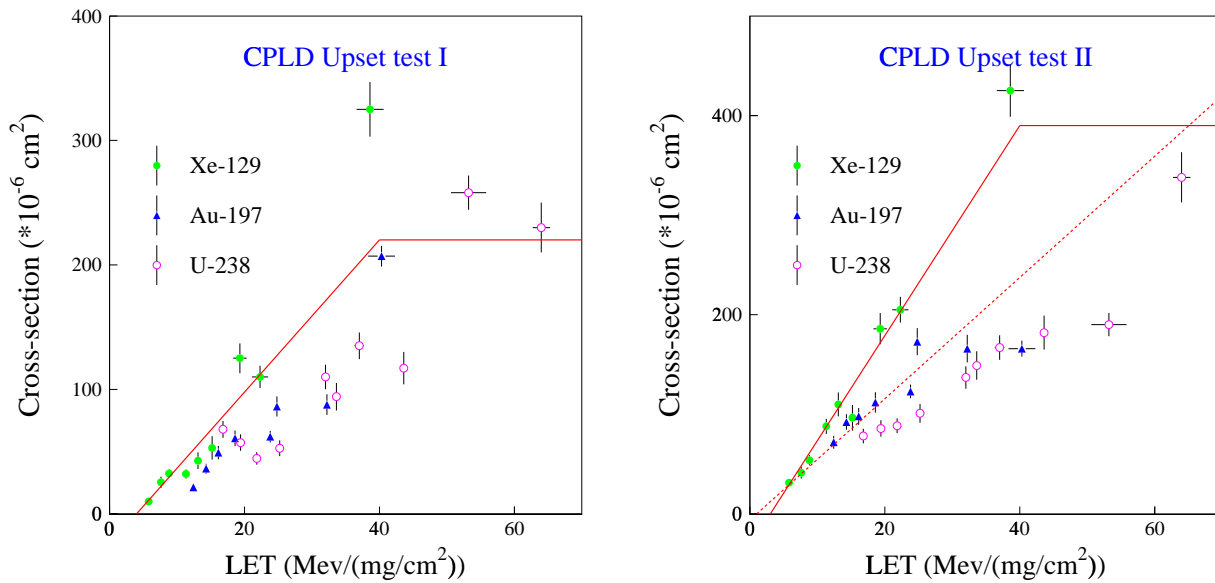


Figure 17: CPLD – SEU rates as measured in GSI for buffer memory upsets (left plot) and for shift register upset (right plot).

Two types of SEU are identified: buffer memory upsets (type I) and shift register upsets (type II). Each of them leads to an abnormal CPLD functioning. If buffer memory upset occurs during the shift (4% probability) both types of upset are detected. Number of upsets is counted by the CLB during a spill and is reported on request to the DAQ PC between spills. Results on the measured SEU cross section are presented in Figure 17.

SEL threshold is found to be approximately $30 \text{ MeV}/(\text{mg}/\text{cm}^2)$, SEU type I threshold is approximately $4 \text{ MeV}/(\text{mg}/\text{cm}^2)$ and SEU type II threshold is approximately $2 \text{ MeV}/(\text{mg}/\text{cm}^2)$. The SEL rate per day on ISS are estimated to be: $(2.0 \pm 0.5) \times 10^{-12}$ for SEL and $(3_{-3}^{+10}) \times 10^{-5}$ for SEU.

10 FLASH memory, MBM29DL324TE

FLASH memory has an on-board latchup protection. It is powered at the beginning of the measurement and switched off only at the end of the measurement. If latchup occurs the Control Logic Box powers off the UUT and generate a corresponding SEL signal. In that case UUT is powered on again at the end of that spill by the DAQ Computer.

Two types of tests are performed: static FLASH tests and dynamic FLASH tests. For the static tests the memory is erased and rewritten before the spill starts and it is read out after the spill ends. For the dynamic tests the same operation is performed several times when chip is being irradiated. Number of upsets of each type is counted by the CLB during a spill and is reported on request to the DAQ PC between spills. Flux calculation is corrected for the UUT power off time.

We distinguish two types of upsets: flip of bits and upset of the control logic resulting in the incomplete memory erase. The feature of the second type is that number of wrong bits approaches the total number of bits.

No bit flips were observed for the static memory tests. Results on upsets in the control logic are presented in Figure 18.

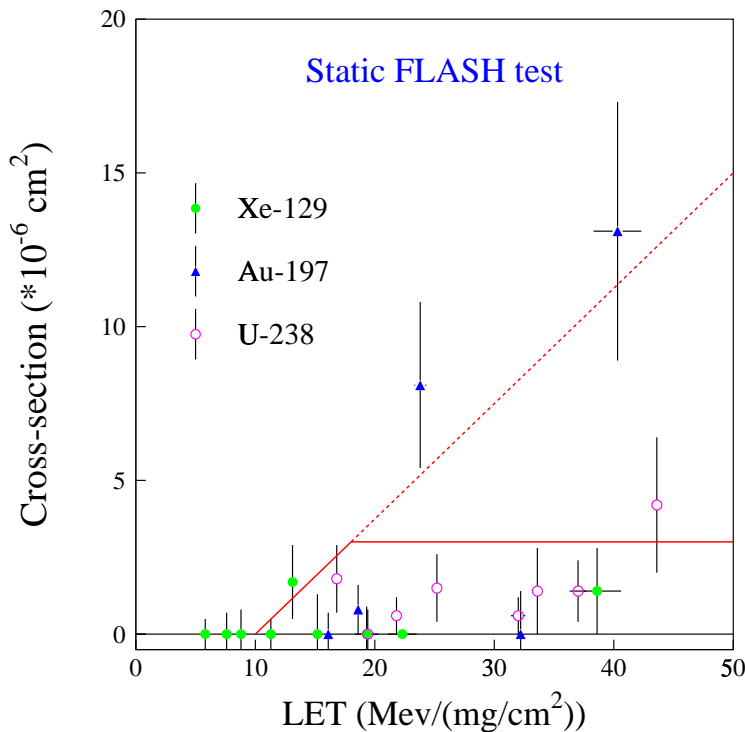


Figure 18: FLASH memory – SEU rates for the static memory tests as measured in GSI.

For the dynamic memory test both effects were observed. It is found that number of bit flips is always a multiple of 4 – this fact is accounted for in the calculation of the statistical error (Figure 19).

No latchups were observed below 23.8 MeV/(mg/cm²) and only few were observed above. The most conservative assumption one can make is that the threshold is 23.8 MeV/(mg/cm²)

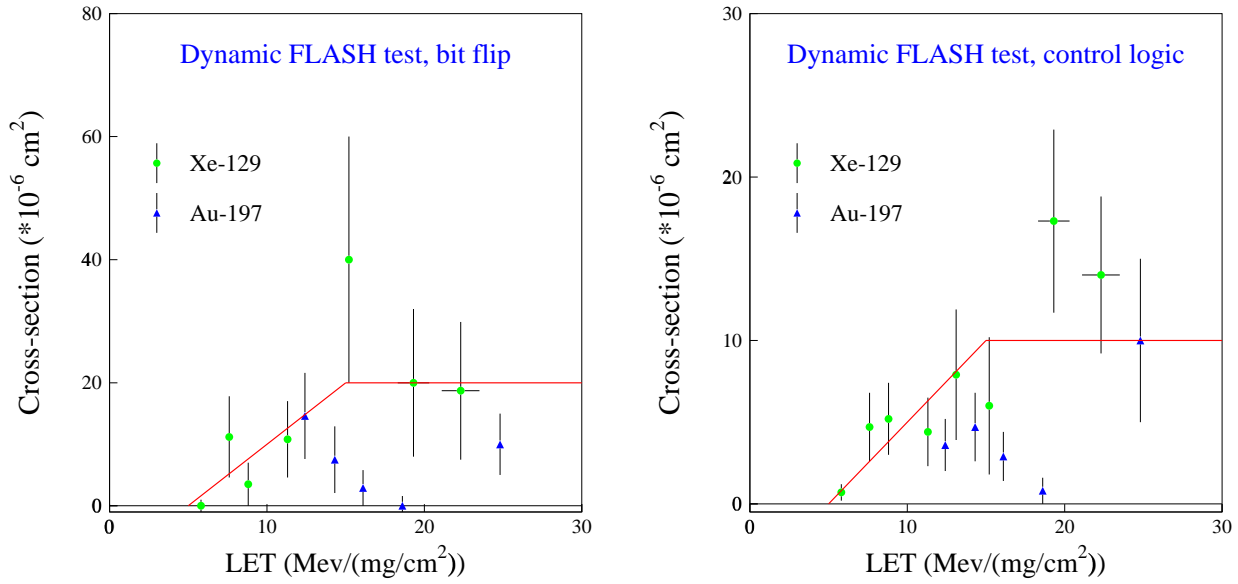


Figure 19: FLASH memory – SEE rates for the static memory tests as measured in GSI. The plot on the left shows the SEU cross section for the bit flips and the plot on the right – cross section for SEU in the control logic.

and the cross section is $2 \times 10^{-5} \text{cm}^2$ above that LET value. This leads to the estimate of the SEL rate per day on ISS to be 10^{-8} .

SEU thresholds are found to be in the range 5 – 10 MeV/(mg/cm²). The SEU rate per day on ISS are estimated to be: 1×10^{-8} for static memory use and $(3.3 \pm 0.9) \times 10^{-7}$ for dynamic memory use.

11 SDRAM memory, MT48LC8M16A2

Perugia SELDP board is used to detect overcurrent, to power off UUT and to generate a corresponding SEL signal. UUT is powered on again at the end of that spill by the DAQ Computer. Results on the SDRAM SEL cross section are presented in Figure 20.

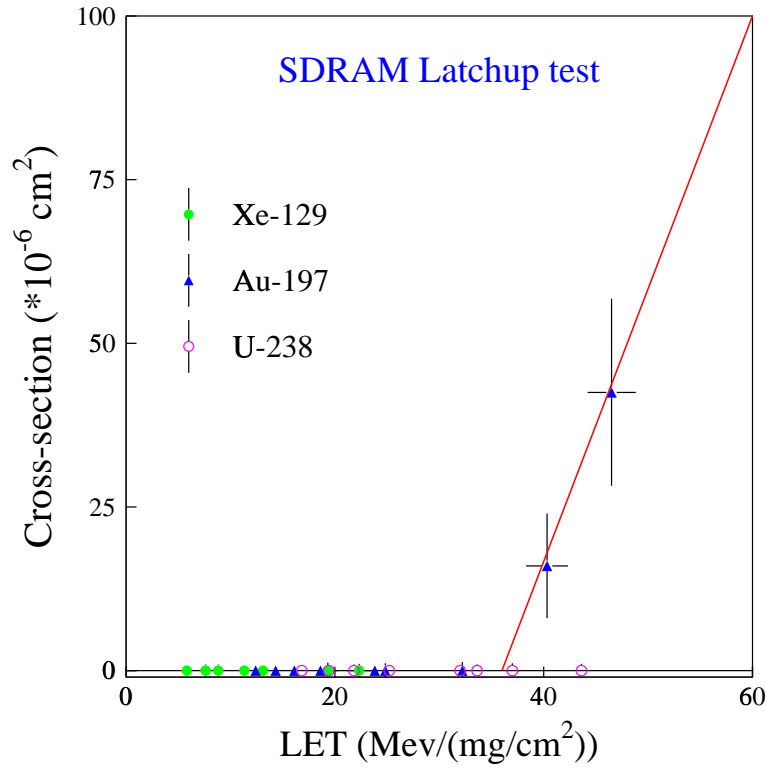


Figure 20: SDRAM – SEL rates as measured in GSI

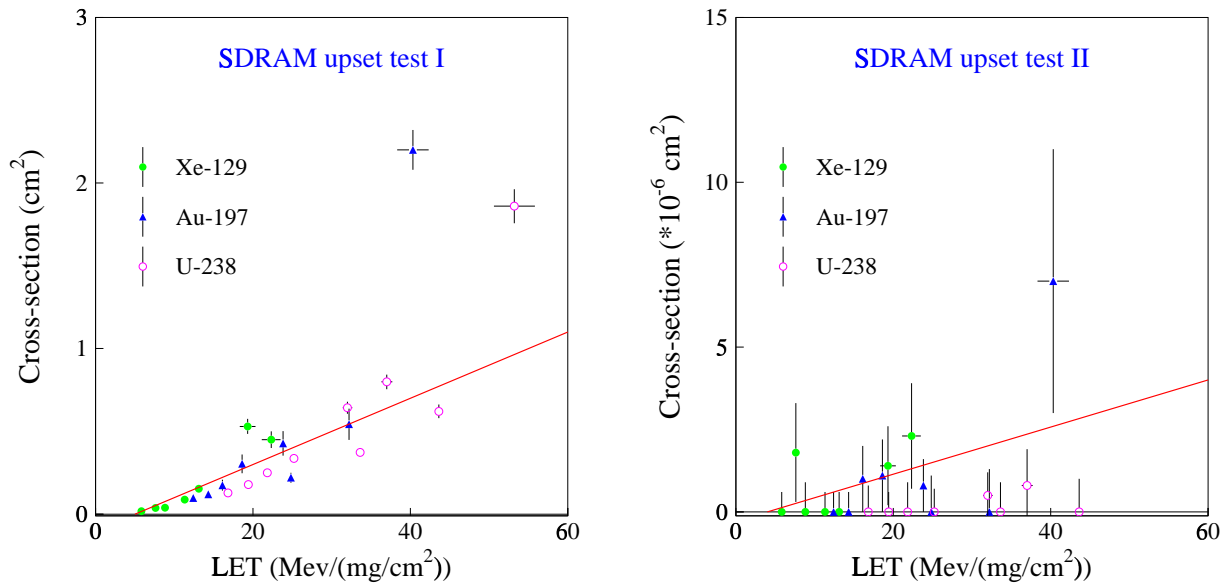


Figure 21: SDRAM – SEU rates as measured in GSI

We distinguish two types of upsets: flip of bits and upset of the control logic leading to a corruption of the operation mode register. The feature of the second type is that the entire memory can not be read or written. Number of upsets of each type is counted by the CLB during a spill and is reported on request to the DAQ PC between spills. Flux calculation is corrected for the UUT power off time. Results on the measured SEU cross section are presented in Figure 21.

SEL threshold is found to be approximately $36 \text{ MeV}/(\text{mg}/\text{cm}^2)$. SEU thresholds are found to be in the range $4 - 5 \text{ MeV}/(\text{mg}/\text{cm}^2)$. The SEE rates per day on ISS are estimated to be: 1×10^{-11} for SEL and $(2.5 \pm 1.0) \times 10^{-3}$ for SEU (1.3×10^{-8} corresponds to the upsets in the control logic).

12 PPC750

PPC750 has an on-board latchup protection. It is powered at the beginning of the measurement and switched off only at the end of the measurement. If latchup occurs the protection circuit cycles the power on the UUT and generates a corresponding SEL signal. Flux counting is inhibited if UUT is not powered. Processor is in the idle state when power is on. Results on the SEL cross section are presented in Figure 22.

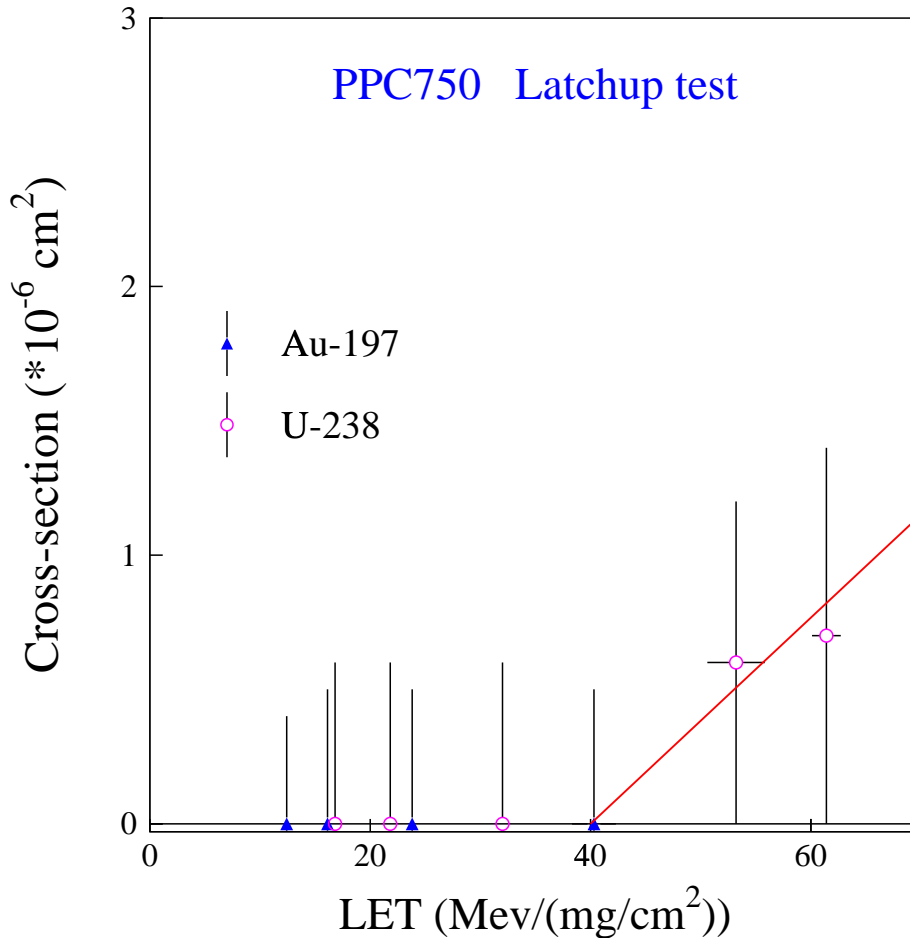


Figure 22: PPC750 – SEL rates as measured in GSI

No upset measurements are performed for the PPC750 chip.

SEL threshold is estimated to be approximately 40 MeV/(mg/cm²). This translates into the SEL rates per day on ISS of 3×10^{-13} .

13 CPC700

CPC700 has an on-board latchup protection. It is powered at the beginning of the measurement and switched off only at the end of the measurement. If latchup occurs the protection circuit cycles the power on the UUT and generates a corresponding SEL signal. Flux counting is inhibited if UUT is not powered. Results on the SEL cross section are presented in Figure 23.

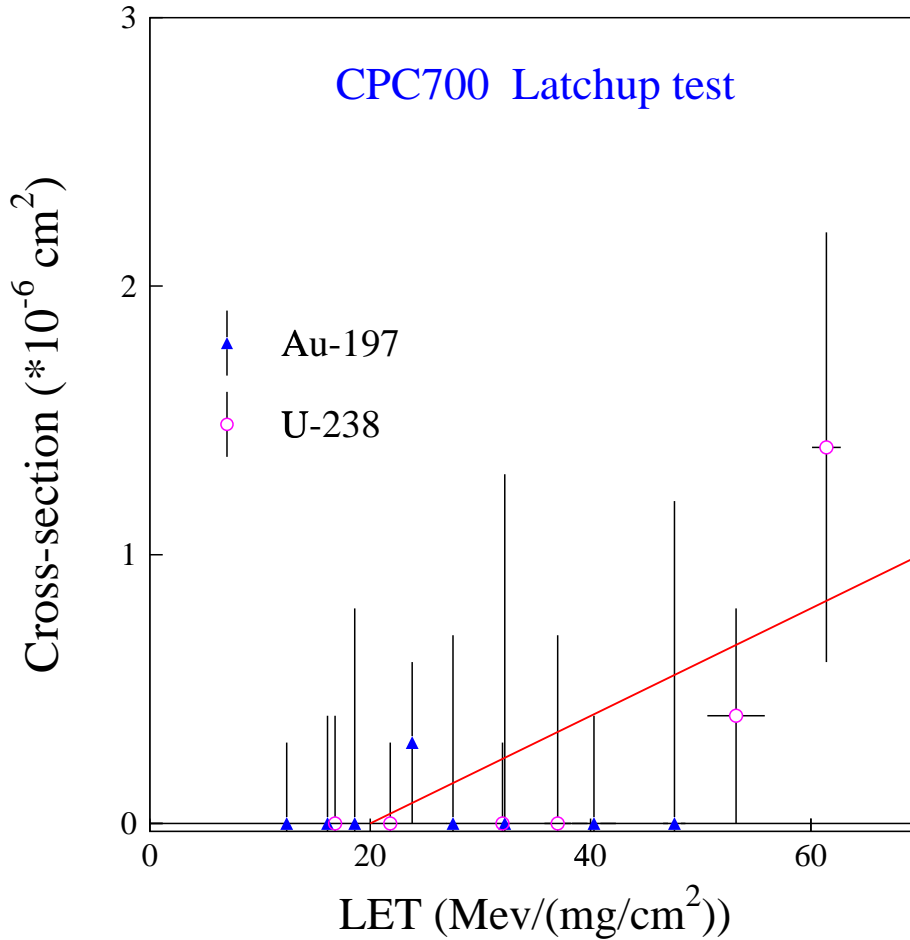


Figure 23: CPC700 – SEL rates as measured in GSI

No upset measurements are performed for the CPC700 chip.

SEL threshold is estimated to be approximately 20 MeV/(mg/cm²). This translates into the SEL rates per day on ISS of 1×10^{-10} .

14 PLX9080

PLX9080 chip has an on-board latchup protection. It is powered at the beginning of the measurement and switched off only at the end of the measurement. If latchup occurs the protection circuit cycles the power on the UUT and generates a corresponding SEL signal. Flux counting is inhibited if UUT is not powered. Results on the SEL cross section are presented in Figure 24.

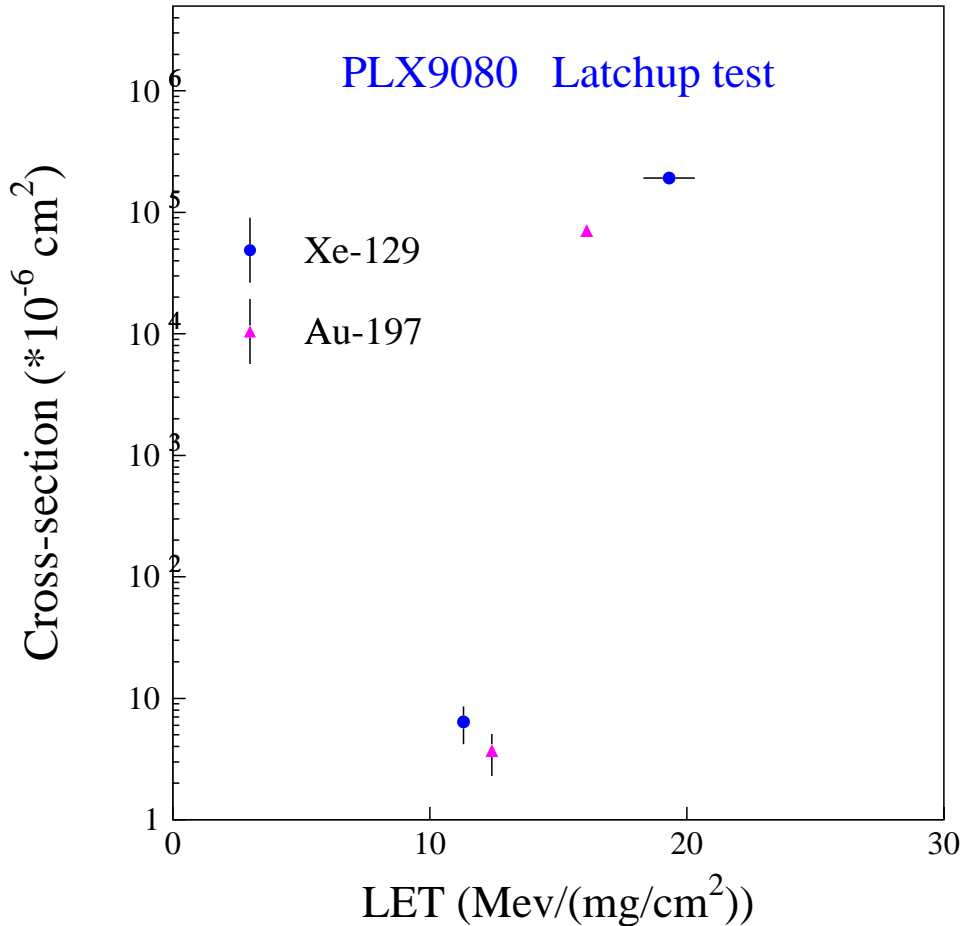


Figure 24: PLX9080 – SEL rates as measured in GSI

No upset measurements are performed for the PLX9080 chip.

SEL threshold is estimated to be approximately 12 MeV/(mg/cm²). However, the cross section grows very rapidly and reaches macroscopic values at 20 MeV/(mg/cm²) (Figure 24). It should be noted that two PLX9080 chips were physically dead after sustaining some 1000 latchups each, what prevents recommending this chip for use in AMS DAQ. Nevertheless, the formal estimate of the SEL rate per day on ISS results in 1×10^{-3} .

15 MHV100

MHV100 chip has an on-board latchup protection. It is powered at the beginning of the measurement and switched off only at the end of the measurement. If latchup occurs the protection circuit cycles the power on the UUT and generates a corresponding SEL signal. Flux counting is inhibited if UUT is not powered. Results on the SEL cross section are presented in Figure 25.

Upset measurements are performed using only spills in which there were no latchups. This limits upset rate measurement to LET range below 20 MeV/(mg/cm²). Results of this analysis are presented in Figure 25.

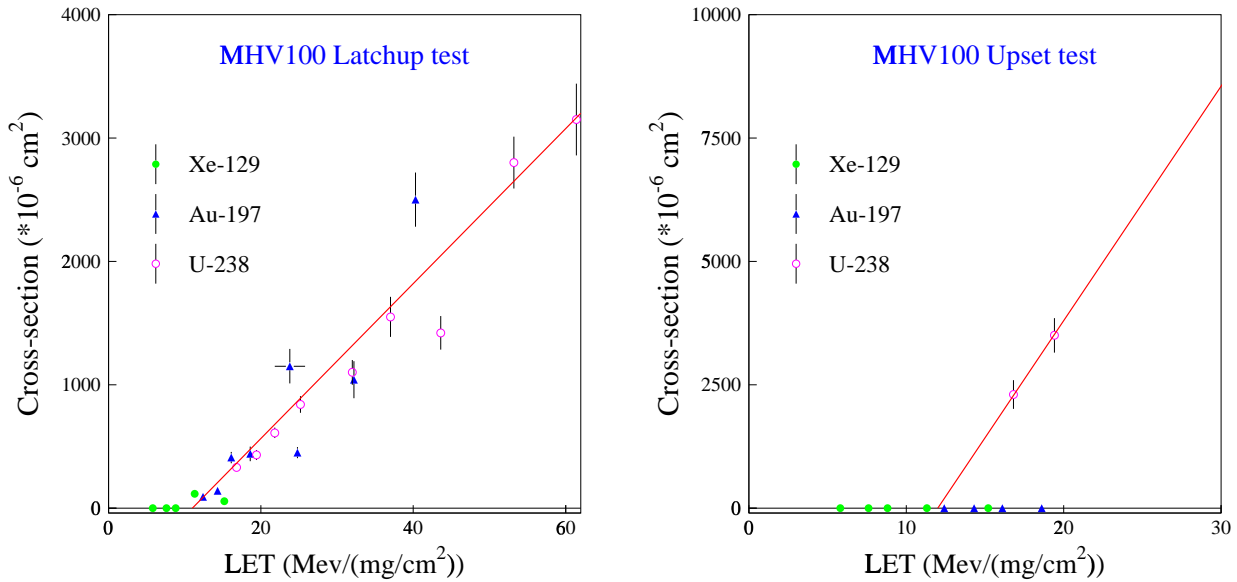


Figure 25: MHV100 – SEE rates as measured in GSI

SEL threshold is measured to be $11 \text{ MeV}/(\text{mg}/\text{cm}^2)$, leading to the SEL rates per day on ISS of $(1.8 \pm 0.8) \times 10^{-6}$. SEU threshold is estimated to be $15 \pm 3 \text{ MeV}/(\text{mg}/\text{cm}^2)$, corresponding to SEU rates per day on ISS of $1.0_{-0.8}^{+10.0} \times 10^{-4}$.

16 ACTEL

ACTEL chip has an on-board latchup protection. It is powered at the beginning of the measurement and switched off only at the end of the measurement. If latchup occurs the protection circuit cycles the power on the UUT and generates a corresponding SEL signal. Results on the SEU cross section are presented in Figure 26.

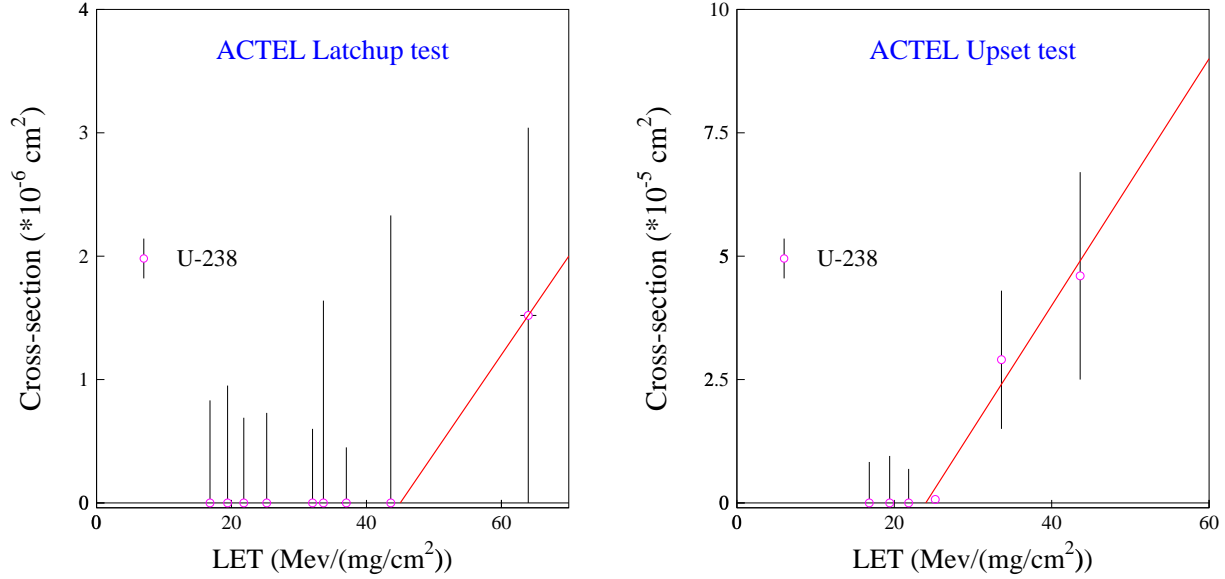


Figure 26: ACTEL – SEE rates as measured in GSI

SEL threshold is measured to be 45 MeV/(mg/cm²), leading to the SEL rates per day on ISS of $(4.1 \pm 1.8) \times 10^{-13}$. SEU threshold is estimated to be 24 MeV/(mg/cm²), corresponding to SEU rates per day on ISS of $2.7 \pm 0.9 \times 10^{-9}$.

17 QLOGIC

QLogic chip has an on-board latchup protection. It is powered at the beginning of the measurement and switched off only at the end of the measurement. If latchup occurs the protection circuit cycles the power on the UUT and generates a corresponding SEL signal. Results on the SEU cross section are presented in Figure 27.

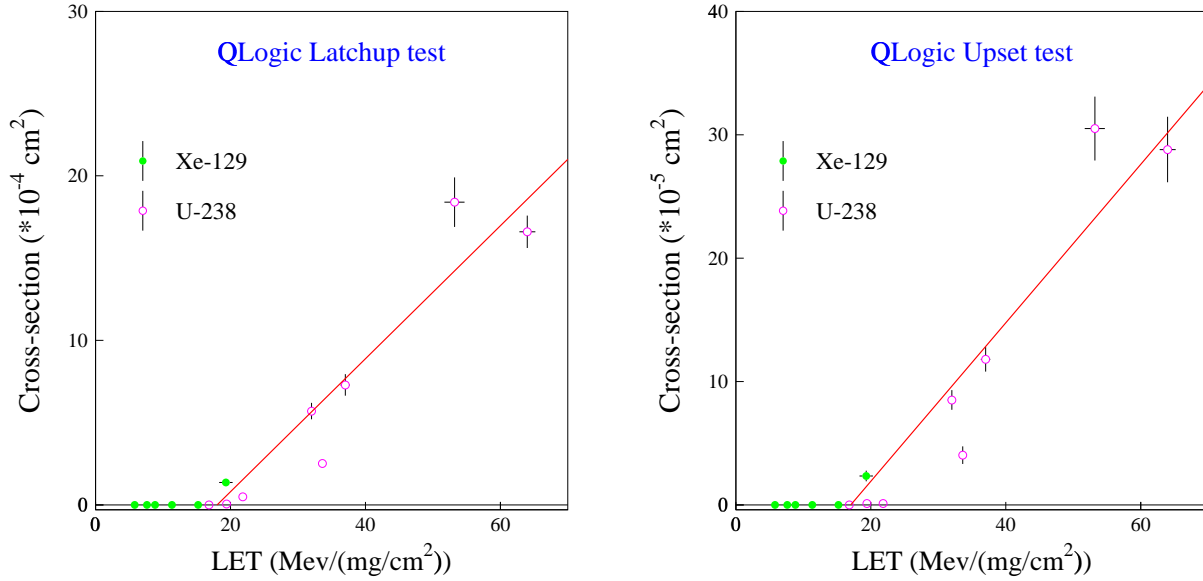


Figure 27: QLogic – SEE rates as measured in GSI

SEL threshold is measured to be $18 \text{ MeV}/(\text{mg}/\text{cm}^2)$, leading to the SEL rates per day on ISS of $(2.7 \pm 0.8) \times 10^{-7}$. SEU threshold is estimated to be $17 \text{ MeV}/(\text{mg}/\text{cm}^2)$, corresponding to SEU rates per day on ISS of $5.3 \pm 1.6 \times 10^{-8}$.

18 USCM controller, DS80C390

DALLAS controller has an on-board latchup protection. It is powered at the beginning of the measurement and switched off only at the end of the measurement. If latchup occurs the protection circuit cycles the power on the UUT and, for runs taken with Au⁷⁹ and U⁹² beams, generates a corresponding SEL signal.

No latchups are observed below LET of 16 MeV/(mg/cm²). However the board failed to function properly for beams with LET above 16 MeV/(mg/cm²). In fact it looked non-operational after first few latchups have occurred. From the performed tests it is not clear whether the malfunctioning is due to the latchup protection circuit or the chip itself. This requires further investigation.

Making a conservative assumption that the latchup threshold is 16 MeV/(mg/cm²) and grows rapidly to the actual chip size above that value, the probability that chip dies is 2×10^{-3} per day on ISS.

19 Conclusions

Most of the components tested at GSI are enough radiation tolerant for use in the AMS DAQ system. It is convenient to summarise the results of the measurements in terms of SEE rate per day on ISS. A word of caution: as we are not sensitive to cross sections below 10^{-7}cm^2 and we did not study the LET region below $5\text{ MeV}/(\text{mg}/\text{cm}^2)$ it is reasonable to compare the expected rates on ISS with the sensitivity limit of $2 \cdot 10^{-6}\text{day}^{-1}$ corresponding to a flat cross section of 10^{-7}cm^2 starting from $1\text{ MeV}/(\text{mg}/\text{cm}^2)$.

The status of results from GSI tests are summarised in Table 2:

Table 2: Estimate of SEE rates per component on ISS.

Component	Part Number	SEL rate (day^{-1})	SEU rate (day^{-1})
DSP	ADSP2187L	$8 \cdot 10^{-8}$	$1 \cdot 10^{-4}$
DSP	ADSP2189M	$2 \cdot 10^{-7}$	$2 \cdot 10^{-4}$
DALLAS controller	DS80C390	$2 \cdot 10^{-3}$	
CPU	PPC750	$3 \cdot 10^{-13}$	-
Host/PCI bridge	CPC700	$1 \cdot 10^{-10}$	-
PCI Adaptor	PLX PCI9080	$1 \cdot 10^{-3}$	-
Watchdog Timer	AMD679	$5 \cdot 10^{-9}$	$4 \cdot 10^{-8}$
CPLD	CY3700	$2 \cdot 10^{-12}$	$3 \cdot 10^{-5}$
SDRAM 128 Mbit	MT48LC8M16A2	$1 \cdot 10^{-11}$	$3 \cdot 10^{-3}$
FLASH memory	MBM29DL324TE	$1 \cdot 10^{-8}$	$3 \cdot 10^{-7}$
HV controller	MHV100	$2 \cdot 10^{-6}$	$1 \cdot 10^{-4}$
PGA	QL12X16BL	$3 \cdot 10^{-7}$	$5 \cdot 10^{-8}$
PGA	Actel 54SX32	$4 \cdot 10^{-13}$	$3 \cdot 10^{-9}$
RICH FE chip	AMS	$4 \cdot 10^{-8}$	$8 \cdot 10^{-8}$
ECAL FE chip	AMS	negl	-
HCC	AMS	$2 \cdot 10^{-7}$	negl
Digital Coupler	ISO150	negl	$5 \cdot 10^{-4}$
Digital Coupler	ADM	$6 \cdot 10^{-9}$	negl
ADC	ADS803U	$3 \cdot 10^{-9}$	$2 \cdot 10^{-7}$
VA32 old		$1 \cdot 10^{-6}$	-
VA32 new		$2 \cdot 10^{-8}$	-

References

- [1] AMS Note DAQ-GSI-1, 12 October 2000.
- [2] SRIM2000 Package – Stopping and Range of Ions in Matter.
- [3] CREME96 Package – Cosmic Ray Effects on Micro Electronics.