

# Study of Single Event effects in electronic components. Part III.

P.Berges, J.Burger, G.Castellini, Y.H.Chang, F.Cindolo, E.Fiori,  
D.Fougeron, P.J.Hong, V.Hermel, A.Koulemzine, A.Kounine,  
V.Koutsenko, C.H.Lin, M.Lolli, J.Marin, M.Menichelli, A.Papi  
V.Plyaskine, R.Simon, D.Schardt, M.Steuer, S.Straulino

## Abstract

Single Event Effects in electronic components are studied using heavy ion beams to probe the LET range from 15.9 to 58 MeV/(mg/cm<sup>2</sup>). Tests are performed at GSI, Darmstadt in May 2002. Single Event Latchup and Upset rates are measured for several commercial-grade components. Results of the measurements are projected to the ISS radiation environment.

**This note is for internal use only.**

Please direct any comments to [Andrei.Kounine@cern.ch](mailto:Andrei.Kounine@cern.ch)

# 1 Introduction

Studies of Single Event Effects in electronic components for AMS-2 detector have been already presented in [1, 2]. In the present note new measurements performed at GSI, Darmstadt in May, 2002 are described.  $U^{92}$  ion beams with energies 100–900 MeV/nucleon were used for these studies:

Table 1: LET and range estimates for  $U^{92}$  beams.

Beam energy (MeV/nucleon)	100	150	200	400	900
$U^{92}$ LET (MeV/mg/cm <sup>2</sup> )	58.0	38.5	32.0	21.8	15.9
$U^{92}$ RNG (mm)	1.6	3.2	4.6	13.0	40.5

Detailed description of the experimental setup and the test procedures, including definition of upsets, can be found on <http://ams.cern.ch/AMS/Beamtest>. This note includes only a brief description of the test results.

## 2 JMDC components

### 2.1 CYPRESS Z9972BA PLL clock driver

CYPRESS Z9972BA PLL clock driver was tested up to 58 (Mev/mg/cm<sup>2</sup>) with no latchup protection. The test is performed using JSBC board. The test program executed by the processor performs three types of operations: execution unit tests (integer and floating point arithmetics); system memory test (to test PLB interface) and L1 Data Cache test. No exceptions are defined in the code. The information on number of errors of different types is readout by DAQ PC from JSBC using RS232 line running at 57.8 Kb/sec.

No destructive effects (SEL) were observed in the entire tested range of LET 15.9–58.0 Mev/mg/cm<sup>2</sup>. We observed only one type of SEU – processor hangs (Figure 1).

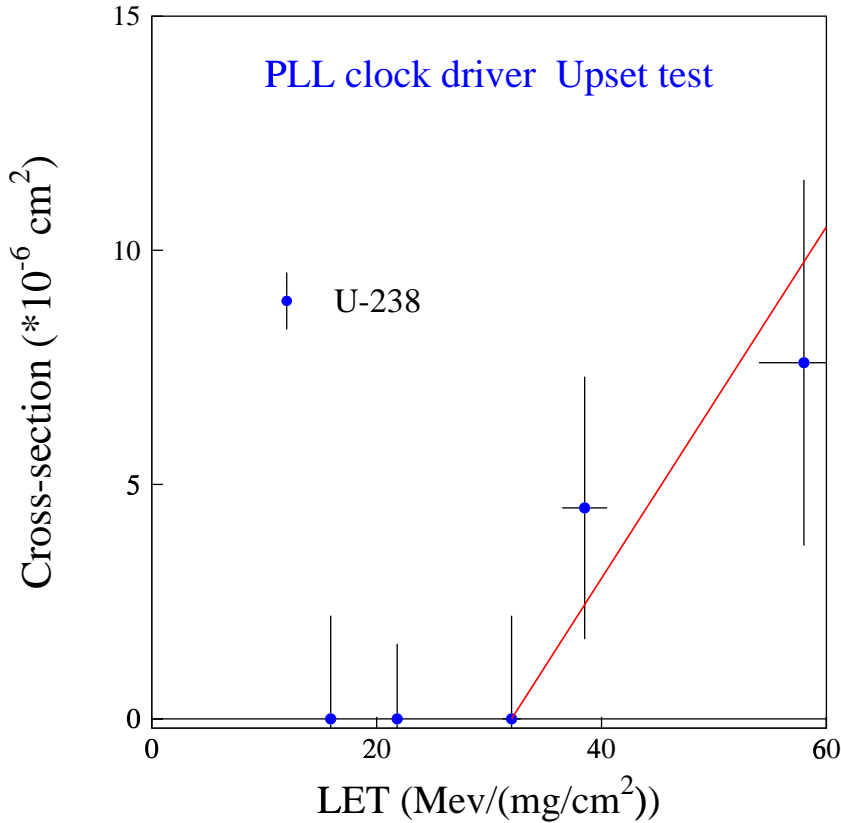


Figure 1: PLL clock driver – SEU rates as measured in GSI

SEU threshold is estimated to be 32 MeV/(mg/cm<sup>2</sup>). This translates into the SEU rates per day on ISS of 10<sup>-11</sup>.

### 2.2 Watchdog timer, MAX706ESA

No SELs were observed in MAX706ESA using 200-500 MeV/nucl U<sup>92</sup> beam with JSBC board. There were no latchup protection circuits on that board. The program executed by the processor is the same as in the PLL clock driver test. The dominant upset type observed is no response (in 0.5 sec) on the RS232 line. The upset rate at 20 MeV/(mg/cm<sup>2</sup>) is estimated to be (1.9 ±

$0.4) \cdot 10^{-4} \text{cm}^2$ . Assuming (conservatively) that SEL threshold is  $30 \text{ MeV}/(\text{mg}/\text{cm}^2)$  and SEU threshold is  $1 \text{ MeV}/(\text{mg}/\text{cm}^2)$ , the SEE rates per day on ISS are estimated to be  $< 1 \times 10^{-7}$  for SEL and  $< 6 \times 10^{-5}$  for SEU.

### 2.3 Linear Voltage regulators.

SHARP PQ7DV10 was tested both using a dedicated board (for SEL) and JSBS board (for SEU). No SEL were observed. Some upsets on the JSBC board were observed only at LET of  $38 \text{ MeV}/\text{mg}/\text{cm}^2$ . They are related to L1 Cache memory corruptions and the rate is measured to be  $(2.0 \pm 1.5) \cdot 10^{-6} \text{cm}^2$  what is at the limit of our sensitivity. This translates into the SEU rates per day on ISS of  $10^{-11}$ .

LM2989A regulator from National is tested using a dedicated board. The output of the regulator –  $2.5\text{V}$  of regulated voltage is loaded onto  $4.7\Omega$  resistor. This voltage is monitored and deviations exceeding 8% for more than 10 ns are counted as upsets. No SEL-protecting circuitry was used for the tests, and DUT was functional in the whole range of probed LETs  $15.9 - 58.0 \text{ MeV}/(\text{mg}/\text{cm}^2)$ .

Only voltage drops are observed during DUT irradiation (no over-voltages) (Figure 2).

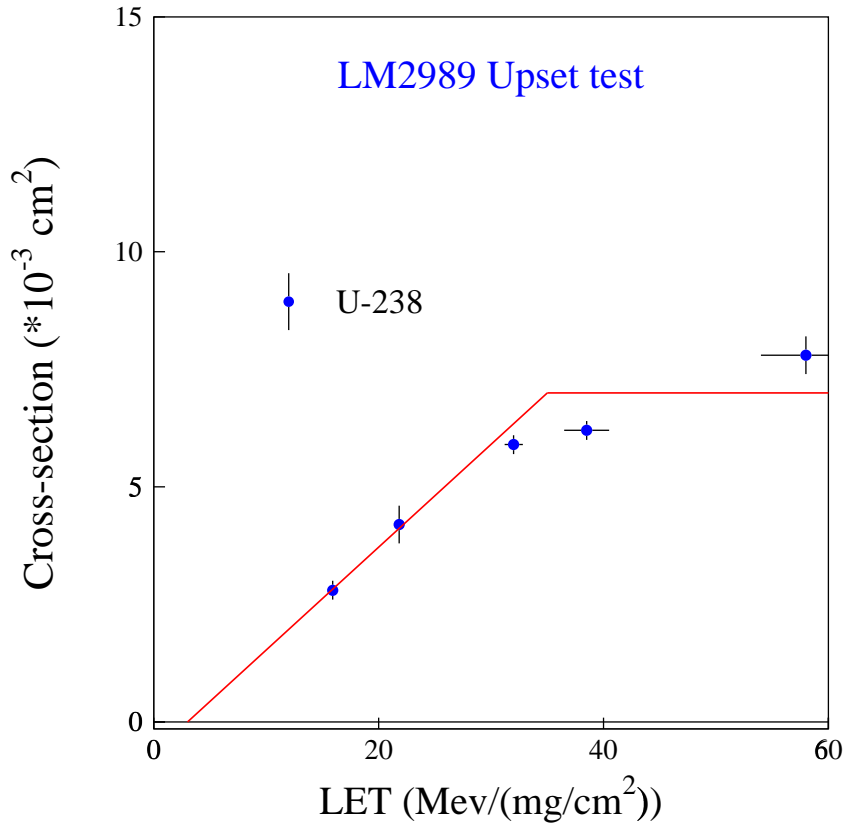


Figure 2: LM2989 – SEU rates as measured in GSI

Extrapolating (conservatively) the SEU threshold to  $3 \text{ MeV}/(\text{mg}/\text{cm}^2)$ , the SEU rate per day on ISS is (over)estimated to be  $6 \times 10^{-5}$ .

## 2.4 STATEK oscillator.

Statek oscillator, CXO3M-10N-50.0M was tested using a dedicated board. Perugia SELDP is used to detect over-current on the input power line, to power off DUT and to generate a corresponding SEL signal. DUT is powered on again at the end of that spill by the DAQ Computer.

As an upset measure the number of clocks generated by the oscillator under test during a spill is compared with the number of clocks generated by a reference unit. The corresponding spectrum of the normalised count difference is presented in Figure 3. No abnormal differences are observed.

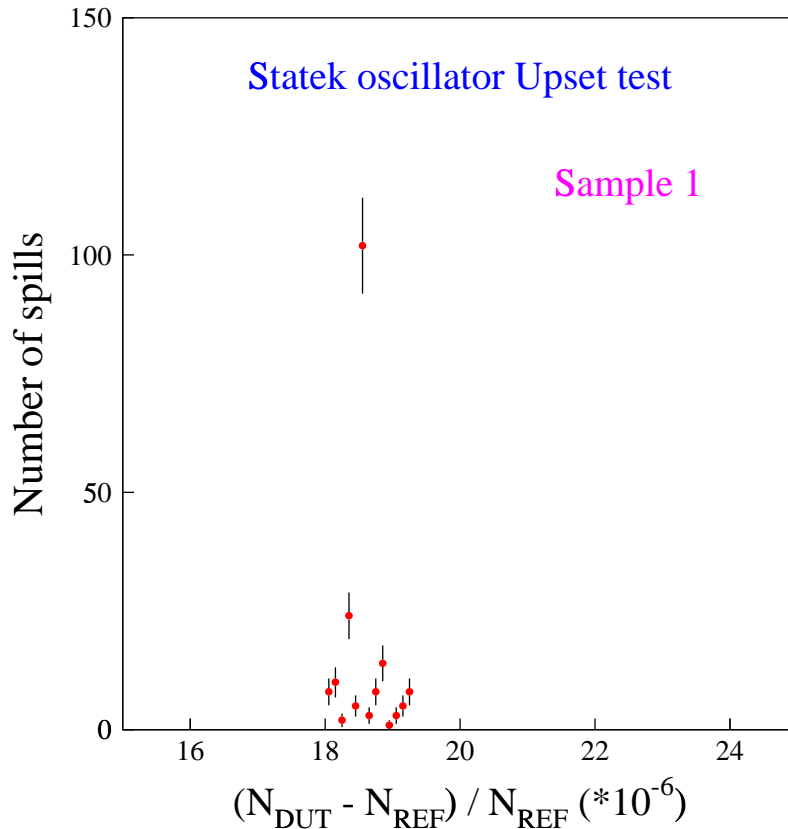


Figure 3: Normalised difference of  $(N_{\text{DUT}} - N_{\text{REF}})/N_{\text{REF}}$ . One entry in the histogram corresponds to one spill of irradiation.

No SEE are observed in the range of LET  $15.9 - 58.0 \text{ MeV}/(\text{mg}/\text{cm}^2)$ , leading to an upper limit estimate for the SEU rate per day on ISS of  $10^{-11}$ .

## 2.5 Transceiver, SN54LVTH16245A

Transceiver, SN54LVTH16245A, is tested using a dedicated board. It is protected against latchups with Perugia SELDP. DUT is powered at the beginning of the measurement and switched off only at the end of the measurement. If latchup is detected SELDP cuts the power on the DUT and generates a corresponding SEL signal. No latchups are observed in the probed LET range  $15.9 - 58 \text{ MeV}/(\text{mg}/\text{cm}^2)$ .

Upset is defined as an error in pattern translation. Pattern change rate is 12 MHz. The measured upset rates are presented in Figure 4.

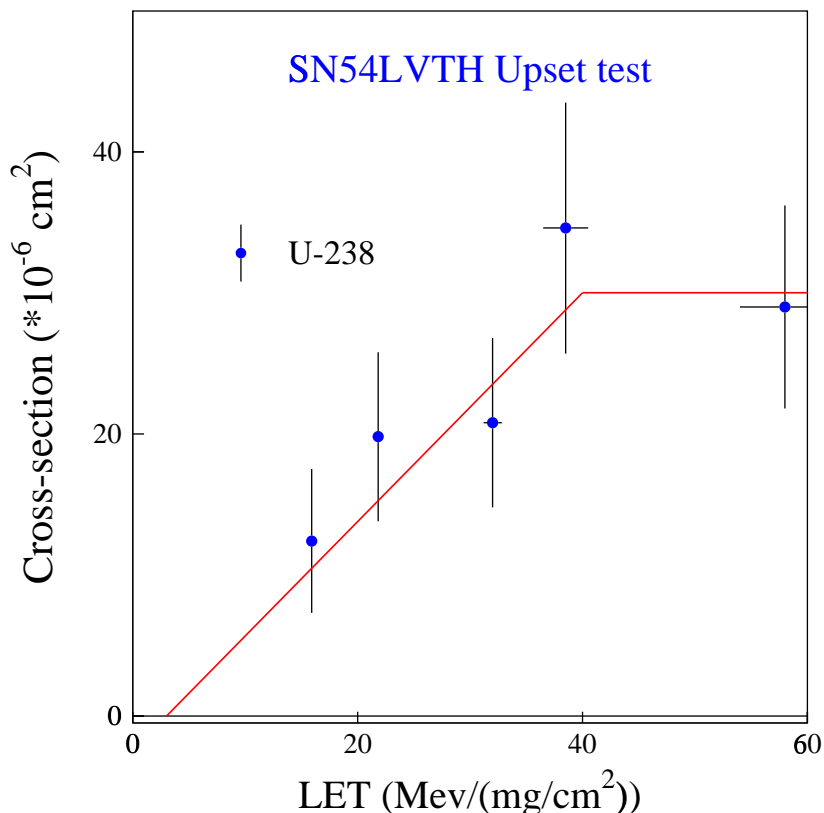


Figure 4: SN54LVTH16245A – SEU rates as measured in GSI.

SEU thresholds is extrapolated to be 3 MeV/(mg/cm<sup>2</sup>). This corresponds to SEU rates per day on ISS of  $2.4 \times 10^{-7}$ .

## 2.6 Level shifter, SN74LVCC3245APW

Level shifter, SN74LVCC3245APW, is tested using a dedicated board. It has an on-board latchup protection circuitry. DUT is powered at the beginning of the measurement and switched off only at the end of the measurement. If latchup is detected SEL detection circuitry cuts the power on the DUT and generates a corresponding SEL signal. Only three latchups are observed at the highest probed LETs of 38.5 and 58.0 MeV/(mg/cm<sup>2</sup>).

Functionality of the component was monitored with a sampling rate of 1.2 KHz. No malfunctioning was observed when the component was powered.

SEL threshold is  $> 32$  MeV/(mg/cm<sup>2</sup>). This results in the estimate of the SEL rate per day on ISS of  $< 10^{-11}$ .

## 2.7 Single Gate buffers, SN74LVC1G\*\*\*

4 Single Gate buffers, SN74LVC1G17DBVR, SN74LVC1G125DBVR, SN74LVC1G126DBVR and SN74LVC1G240DBVR, are tested using a dedicated board, which has an on-board latchup

protection circuitry. DUTs are powered at the beginning of the measurement and switched off only at the end of the measurement. If latchup is detected SEL detection circuitry cuts the power on the DUTs and generates a corresponding SEL signal. Only few latchups are observed at the highest probed LETs of 32.0 and 38.5 MeV/(mg/cm<sup>2</sup>).

Functionality of the component was monitored with a sampling rate of 1.2 KHz. No malfunctioning was observed when the component is powered.

SEL threshold is estimated to be 20 MeV/(mg/cm<sup>2</sup>). The estimate of the SEL rate per day on ISS is  $4 \times 10^{-9}$ .

## 2.8 SDRAM memory, K4S560832C-TL75

SAMSUNG memory, K4S561632C-TL75, is tested using a dedicated board. It is protected against latchups with Perugia SELDP. DUT is powered at the beginning of the measurement and switched off only at the end of the measurement. If latchup is detected SELDP cuts the power on the DUT and generates a corresponding SEL signal. No latchups are observed in the probed LET range 15.9 – 58 MeV/(mg/cm<sup>2</sup>).

We distinguish two types of upsets: flip of bits (Upset I) and upset of the control logic leading to a corruption of the operation mode register (Upset II). The feature of the second type is that the entire memory can not be read or written. Results of the SDRAM SEU cross section measurements are summarised in Figure 5.

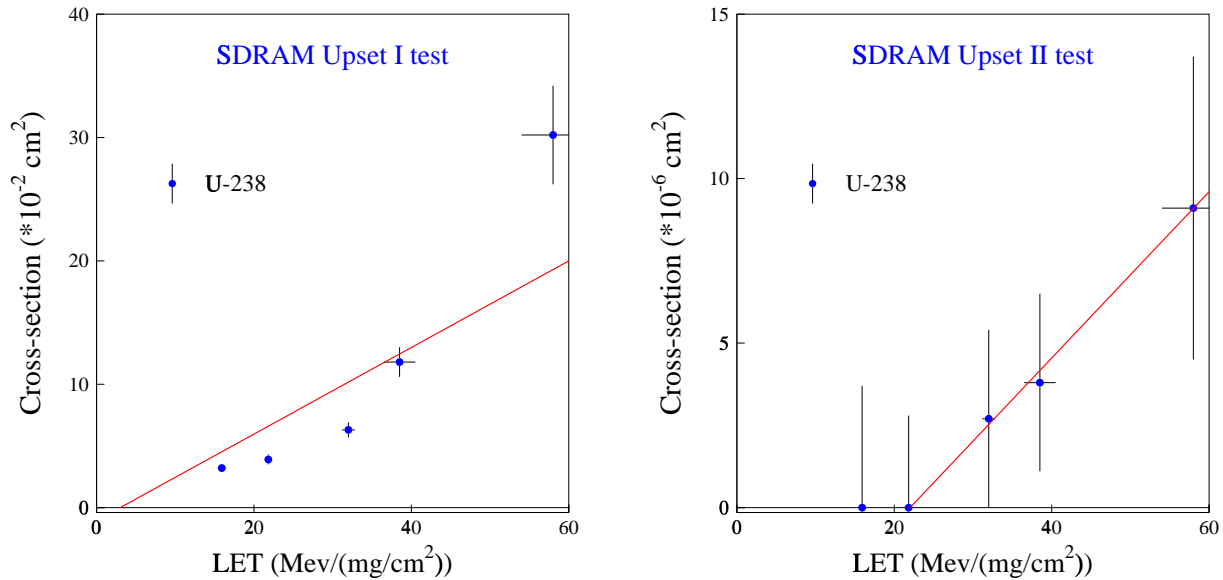


Figure 5: SAMSUNG SDRAM memory – SEU rates as measured in GSI.

These results are compatible with the previous measurements [2]. SEU threshold is extrapolated to be 3 MeV/(mg/cm<sup>2</sup>). This corresponds to SEU rates per day on ISS of  $1.5 \times 10^{-3}$ .

## 2.9 LVDS RX/TX, SN65LVDS391PW/SN65LVDT390PW

LVDS receivers and transmitters are tested using a dedicated board which has an on-board latchup protection circuitry. DUTs are powered at the beginning of the measurement and switched off only at the end of the measurement. If latchup is detected SEL detection circuitry

cuts the power on the DUTs and generates a corresponding SEL signal. No latchups are observed in the probed LET range 15.9–58.0 MeV/(mg/cm<sup>2</sup>).

Functionality of the component was monitored with a sampling rate of 1.2 KHz. No malfunctioning was observed when the component is powered. SEL threshold is > 40 MeV/(mg/cm<sup>2</sup>). This results in the estimate of the SEL rate per day on ISS of < 10<sup>-11</sup>.

### 3 DC/DC MOSFETS

Four MOSFET transistors are tested using a dedicated board. No over-current protection is possible for this type of devices. Therefore DUT is powered at the beginning of the measurement and switched off only when it breaks or the measurement succeeds. Each measurement, which corresponds to single beam energy, was conducted in the following manner:

- first, 38V is applied to the component and about 700000 ions are collected, provided the component is functioning;
- next, 68V is applied to the component and about 700000 ions are collected, provided the component is still functioning;
- last, 96V is applied and about 700000 ions are collected, provided the component is still functioning

With no exception, a component breaks (i.e. a gate rupture/burn-out occurs) in the very first spill which corresponds to highest LET/Voltage attained. If a component withstands the first spill at a given LET/Voltage, it withstands also all consecutive spills at that LET/Voltage. Therefore if component passes a test at a given LET/Voltage one can only derive an upper limit on a gate rupture cross-section. However, if destructive effect occurs it is not possible to estimate a correct flux for the cross section calculation. Therefore in the event of gate rupture/burn-out the cross section assumed to be equal to the chip area:  $\sim 0.1\text{cm}^2$ .

Table 2: SEE cross-section estimates as measured in GSI.

LET/Voltage	FDD2570	IRFR18N15D	FDD3670	HUF76629D3S
15.9/38.0	$< 4.0 \cdot 10^{-6}$	$< 4.0 \cdot 10^{-6}$	$4.0 \cdot 10^{-6}$	$4.0 \cdot 10^{-6}$
15.9/68.0	$< 4.0 \cdot 10^{-6}$	$< 4.0 \cdot 10^{-6}$	$4.0 \cdot 10^{-6}$	$4.0 \cdot 10^{-6}$
15.9/96.0	$< 4.0 \cdot 10^{-6}$	$< 4.0 \cdot 10^{-6}$	0.1	0.1
21.8/38.0	$< 4.0 \cdot 10^{-6}$	$< 4.0 \cdot 10^{-6}$		
21.8/68.0	$< 4.0 \cdot 10^{-6}$	$< 4.0 \cdot 10^{-6}$		
21.8/96.0	$< 4.0 \cdot 10^{-6}$	$< 4.0 \cdot 10^{-6}$		
32.0/38.0			0.1	
38.5/38.0	$< 4.0 \cdot 10^{-6}$	0.1		
38.5/68.0	0.1			

Results of all measurements are summarised in Table 2. Given the numbers one may estimate the per day probability that a component will be destroyed on ISS: FDD3670 and HUF76629D3S – 0.0002 (i.e. will be destroyed during the flight); FDD2570 and IRFR18N15D operating at > 40V –  $7.5 \times 10^{-5}$ ; and FDD2570 operating at < 40V –  $7.2 \times 10^{-8}$ . Upon these results only FDD2570 operating at < 40V can be recommended for use in AMS. For operating at at a nominal voltage of 60V there are two candidates requiring more studies: FDD2570 and IRFR18N15D.

## 4 Tracker components

Several components to be used in the tracker power supply system were tested using dedicated boards. The list comprises: operational amplifiers, AD8052, LM158AH, LM158D, LM258, LM6142; ADC, MAX1281; voltage reference, LM4040; comparators, LM139AD, LM239AD; and custom SELP ASIC chip.

All test boards are protected against latchups with Perugia SELDP. DUT is powered at the beginning of the measurement and switched off only at the end of the measurement. If latchup is detected SELDP cuts the power on the input power line and generates a corresponding SEL signal.

Upsets were not studied for the Tracker components.

No latchups are observed for all components, but LM6142. The latchup cross section for LM6142 is presented in Figure 6.

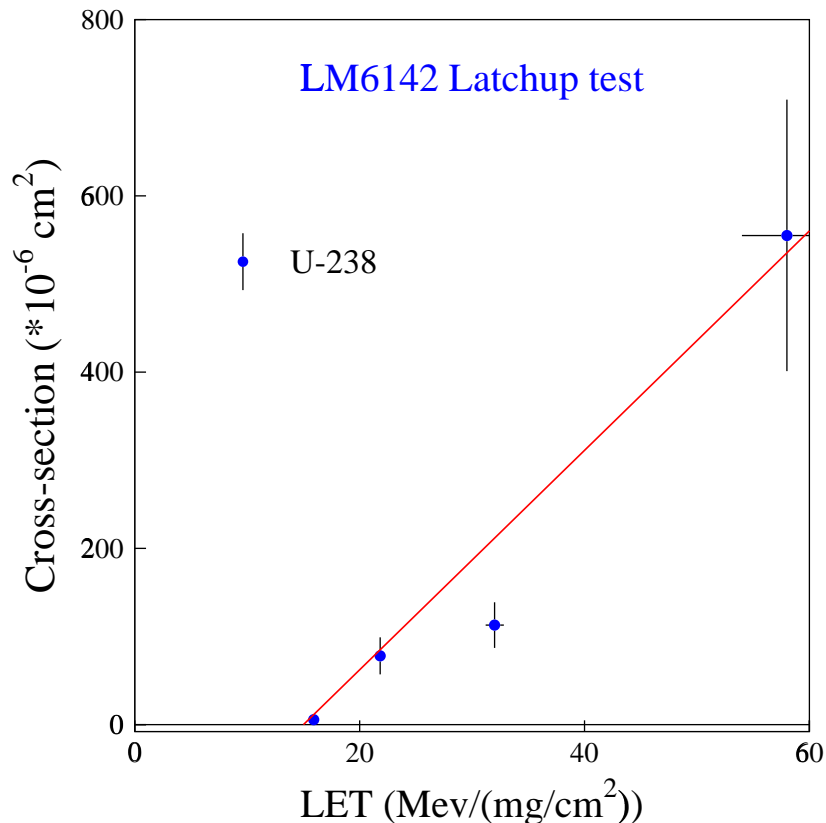


Figure 6: LM6142 – SEL rates as measured in GSI.

For LM6142 an estimate of the SEL rate per day on ISS is  $2 \times 10^{-7}$ , for other tested components it is  $< 10^{-11}$ .

## 5 TRD components

### 5.1 DMOP switch, PHC2300

DMOP switch, PHC2300, is tested using a dedicated board which has an on-board latchup protection circuitry. DUT is powered at the beginning of the measurement and switched off only at the end of the measurement. If latchup is detected SEL detection circuitry cuts the power on the DUTs and generates a corresponding SEL signal. One fatal latchup is observed at the highest probed LET of  $58.0 \text{ MeV}/(\text{mg}/\text{cm}^2)$  (in the second PHC2300 sample).

Functionality of the component was monitored with a sampling rate of 50 Hz. Malfunctioning was observed only with the first PHC2300 sample at  $58.0 \text{ MeV}/(\text{mg}/\text{cm}^2)$ .

SEL threshold is  $> 40 \text{ MeV}/(\text{mg}/\text{cm}^2)$ . This results in the estimate of the SEL rate per day on ISS of  $< 10^{-11}$ .

### 5.2 MOSFET Driver, TPS2814

MOSFET Driver, TPS2814, is tested using a dedicated board which has an on-board latchup protection circuitry. DUT is powered at the beginning of the measurement and switched off only at the end of the measurement. If latchup is detected SEL detection circuitry cuts the power on the DUTs and generates a corresponding SEL signal. One latchup is observed at the highest probed LET of  $58.0 \text{ MeV}/(\text{mg}/\text{cm}^2)$ .

Functionality of the component was monitored with a sampling rate of 50 Hz. Some malfunctioning is observed at 38.5 and at  $58.0 \text{ MeV}/(\text{mg}/\text{cm}^2)$ .

SEL threshold is  $> 40 \text{ MeV}/(\text{mg}/\text{cm}^2)$ . This results in the estimate of the SEL rate per day on ISS of  $< 10^{-11}$ .

## 6 EMC Front-End custom chip

EMC Front-End ASIC is tested using a dedicated board. It is protected against latchups with Perugia SELDP. DUT is powered at the beginning of the measurement and switched off only at the end of the measurement. If latchup is detected SELDP cuts the power on the DUT and generates a corresponding SEL signal. No latchups are observed in the probed LET range  $15.9 - 58 \text{ MeV}/(\text{mg}/\text{cm}^2)$ .

SEL threshold is  $> 40 \text{ MeV}/(\text{mg}/\text{cm}^2)$ . This results in the estimate of the SEL rate per day on ISS of  $< 10^{-11}$ .

## 7 RICH components

Several components to be use in the tracker power supply system were tested using dedicated boards. The list comprises: voltage reference, LM4120; TTL driver, LVT16244; positive voltage regulator, MAX1792; and negative voltage regulator, MAX1735.

All test boards are protected against latchups with Perugia SELDP. DUT is powered at the beginning of the measurement and switched off only at the end of the measurement. If latchup is detected SELDP cuts the power on the input power line and generates a corresponding SEL signal. Functionality of the components was constantly monitored with a sampling rate of 50 Hz.

No latchups were observed for voltage reference, LM4120. It was observed that reference voltage is not stable during the irradiation, however it stabilises immediately when beam is off. The effect does not depend on beam energy, it is the same for the entire probed LET range 15.9 – 58 MeV/(mg/cm<sup>2</sup>).

No latchups and no malfunctioning was observed for the TTL driver, LVT16244.

No latchups were observed for positive voltage regulator, MAX1792. It was observed that regulated voltage is not stable during the irradiation, however it stabilises immediately when beam is off. The effect does not depend on beam energy, it is the same for the entire probed LET range 15.9 – 58 MeV/(mg/cm<sup>2</sup>).

Some latchups are observed for the negative voltage regulator, MAX1735. However the regulated voltage is more stable during the irradiation compared to positive voltage regulator, MAX1792. Only few instabilities were observed for LETs > 21.8 MeV/(mg/cm<sup>2</sup>). The measured SEL cross-section is presented in Figure 7. SEL threshold is > 20 MeV/(mg/cm<sup>2</sup>), it results in the estimate of the SEL rate per day on ISS of < 10<sup>-11</sup>.

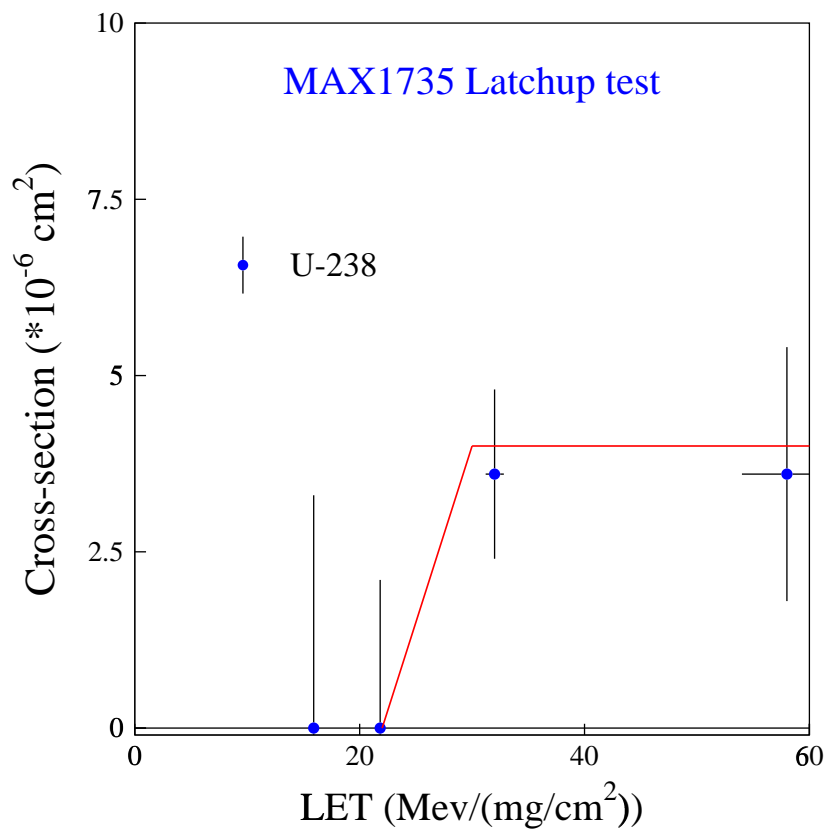


Figure 7: MAX1735 – SEL rate as measured in GSI.

## 8 TOF TDC, LeCroy MTO135-9639

TOF TDC, LeCroy MTO135-9639, is tested using a dedicated board. It is protected against latchups with Perugia SELDP. DUT is powered at the beginning of the measurement and switched off only at the end of the measurement. If latchup is detected SELDP cuts the power on the DUT and generates a corresponding SEL signal. Two LETs were probed – 15.9 and 21.8 MeV/(mg/cm<sup>2</sup>). No latchups are observed at 15.9 and only one at 21.8 MeV/(mg/cm<sup>2</sup>). Upset rate was at the limit of the sensitivity (i.e. cross-section <  $5 \times 10^{-5}$  cm<sup>2</sup>).

SEL threshold is estimated to be 25 MeV/(mg/cm<sup>2</sup>). Assuming macroscopic cross-section at this threshold gives a conservative upper limit on the SEL rate per day on ISS of  $5 \times 10^{-4}$ .

## 9 Conclusions

Most of the components tested at GSI are enough radiation tolerant for use in the AMS DAQ system. Special attention should be paid to MOSFET transistors and for TOF TDC for which more tests may be needed. It is convenient to summarise the results of the measurements in terms of SEE rate per component per day on ISS as done in Table 3:

Table 3: Estimates of SEE rates per component per day on ISS.

Component	SEL rate (day <sup>-1</sup> )	SEU rate (day <sup>-1</sup> )
Z9972BA	immune	$1 \times 10^{-11}$
MAX706ESA	$< 1 \times 10^{-7}$	$< 6 \times 10^{-5}$
PQ7DV10	immune	$1 \times 10^{-11}$
LM2989	immune	-
CXO3M-10N-50.0M	immune	-
SN54LVTH16245A	immune	$2 \times 10^{-7}$
SN74LVCC3245	$1 \times 10^{-11}$	-
SN74LVC1G***	$4 \times 10^{-9}$	-
K4S561632C-TL75	immune	$1.5 \times 10^{-3}$
SN65LVDS391	immune	-
SN65LVDT390	immune	-
<b>FDD2570</b>	$< 1 \times 10^{-4}$	-
<b>IRFR18N15D</b>	$< 1 \times 10^{-4}$	-
<b>FDD3670</b>	$2 \times 10^{-4}$	-
<b>HUF76629D3S</b>	$2 \times 10^{-4}$	-
AD8052	immune	-
LM158AH	immune	-
LM158D	immune	-
LM258	immune	-
LM6142	$2 \times 10^{-7}$	-
MAX1281	immune	-
LM4040	immune	-
LM139AD	immune	-
LM239AD	immune	-
SELP ASIC	immune	-
PHC2300	$1 \times 10^{-11}$	-
TPS2814	immune	-
EMCFE ASIC	immune	-
LM4120	immune	-
LVT16244	immune	-
MAX1792	immune	-
MAX1735	$1 \times 10^{-11}$	-
<b>MTO135-9639</b>	$< 5 \times 10^{-4}$	$< 1 \times 10^{-5}$

## References

- [1] AMS Note 2001-10-01, 8 July 2001.
- [2] DAQ-GSI-3, 15 January 2002.