

AMS WIRE

AMS-II DAQ LINK PROTOCOL

Ver 3.0

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for

AMS DAQ group

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Introduction

- AMS Wire :

- Serial point-to-point link protocol.

- For DAQ links between different level DAQ modules.

- The signaling technique, the data encode method and the character definition are modified from :

- IEEE 1355-1995

- SPACE WIRE Standard Draft D.



Introduction

- Two dedicated buffers for TX and RX.
 - buffer size = Max packet length (e.g. 2 kBytes)

- Master – Slave concept :
 - A slave shall not send any reply out unless it receives a request from any of its masters.
 - High Level Flow Control.



Signaling Technique

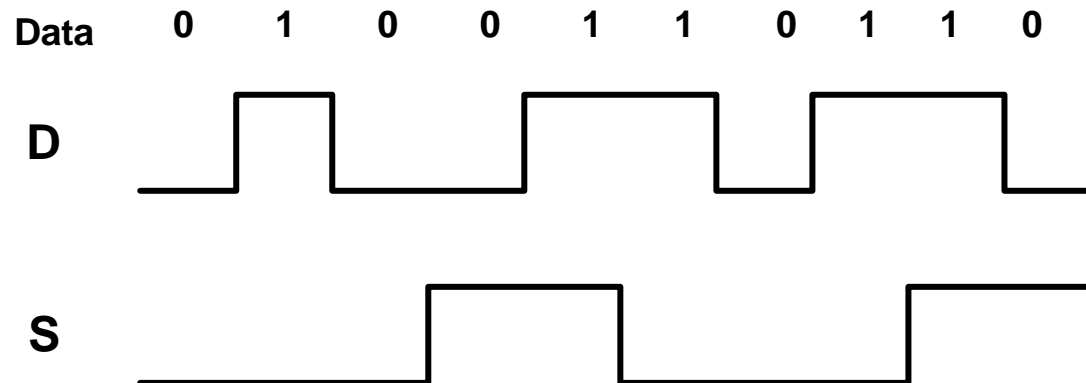
- LVDS : Low Voltage differential signaling
 - ➔ For signals transmitted through a **cable**, across a PCB or along a backplane.

- DS-SE : Single-ends Electrical Transmission (IEEE 1355)
 - ➔ For signals transmitted across a **PCB** or along a **backplane**.

Data Encoding

□ Data/Strobe Encoding (DS) :

- The data values are transmitted directly.
- The strobe signal changes state whenever the data remains constant from one bit to the next.





GAP & Data Rate

- GAP :

- A static state.

- Both D and S signals are high for 8 CLKs.

- Data Rate :

- 100 Mbps.

- Fixed for both directions.

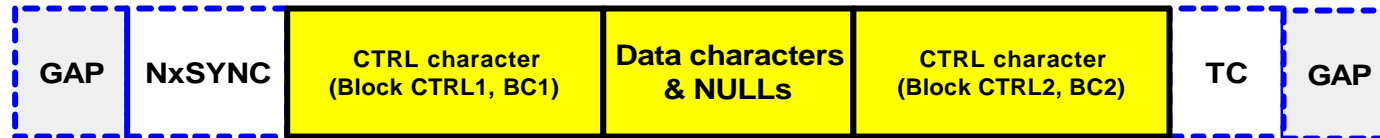


POWER ON and Reset

- LVDS receiver output will be high for all fail-safe conditions (open inputs, terminated inputs and shorted inputs).
 - ➔ After Power on and Reset, the TX shall hold both the data and strobe wires high.
 - ➔ The RX of FE is in "open inputs" condition most of time.

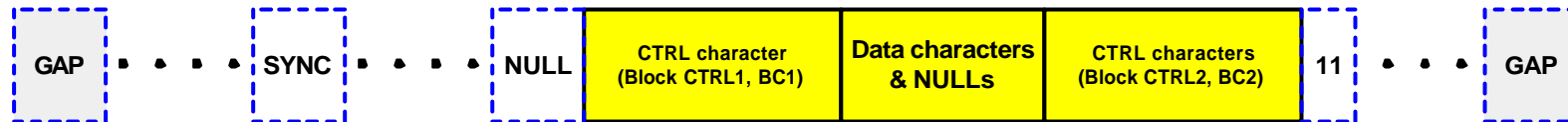
- After GAP, the first bit to be transmitted is "0".
 - ➔ First transition is on the data wire.

Packet Format - TX



- ❑ **The transmission of each packet starts and ends with a GAP.**
- ❑ After GAP, N x SYNCs (N=2) are sent to establish the synchronization.
- ❑ A CTRL char is sent before transmitting any data chars (BC1).
A CTRL char is sent after transmitting all data chars (BC2).
- ❑ **TC : allow a smooth transition from CTRL char to GAP.**

Packet Format - RX



- ❑ One GAP and one SYNC are required before receiving any characters
- ❑ After a SYNC is seen :
 - ➔ SYNC will be identified as the NULL characters.
 - ➔ The NULL is ignored.
- ❑ Before receiving the CTRL char (BC1), only the NULL char is allowed.
- ❑ After the last CTRL char (BC2) is received and checked, the RX shall ignore the incoming characters and wait for a GAP.

Character Definition

Data Characters

←P0XXXX XXXX (MSB first)

Control Characters

←P101	C1	CTRL 1
←P110	C2	CTRL 2
←P100	FCT	Not used
←P111	ESC	Not used
←P111P100		NULL

Special bit patterns

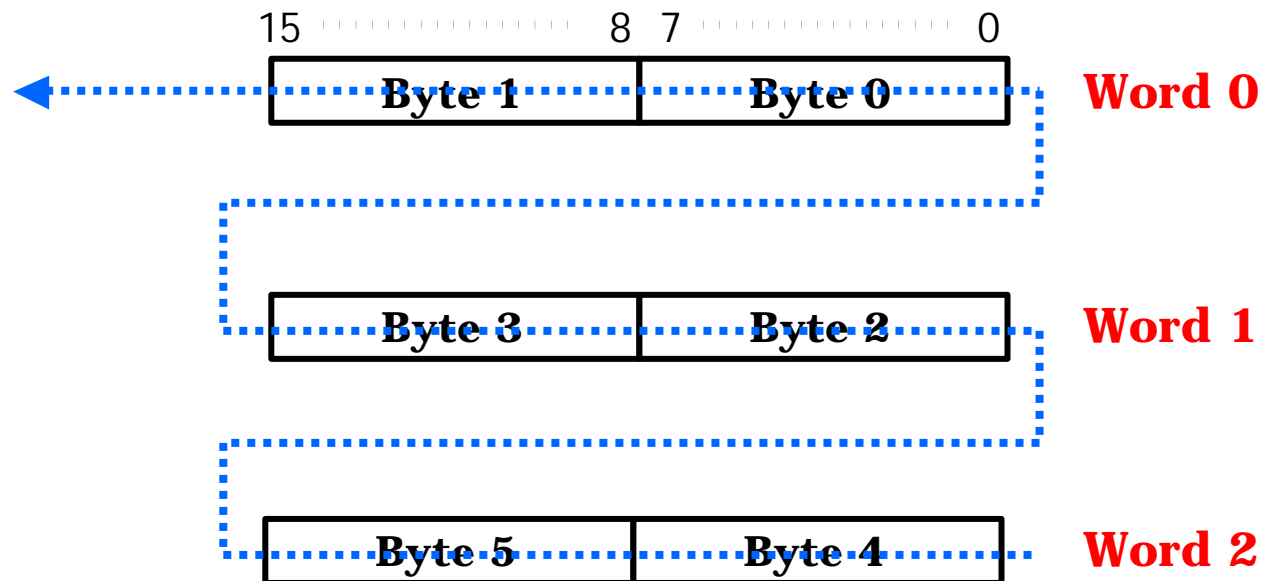
←01110100	SYNC	Synchronization
←11110111	TC	Termination

- Data char : 1 parity bit, 1 flag ("0") and 8 data bits.
- CTRL char : 1 parity bit, 1 flag ("1") and 2 data bits.
- Parity : The total of 1's is an odd number
- SYNC : Establish the synchronization in the beginning of transmission.
- TC : For the termination of transmission.
 - After TC is sent, both the D and S signals are high.
 - A character before TC must be C1 or C2.



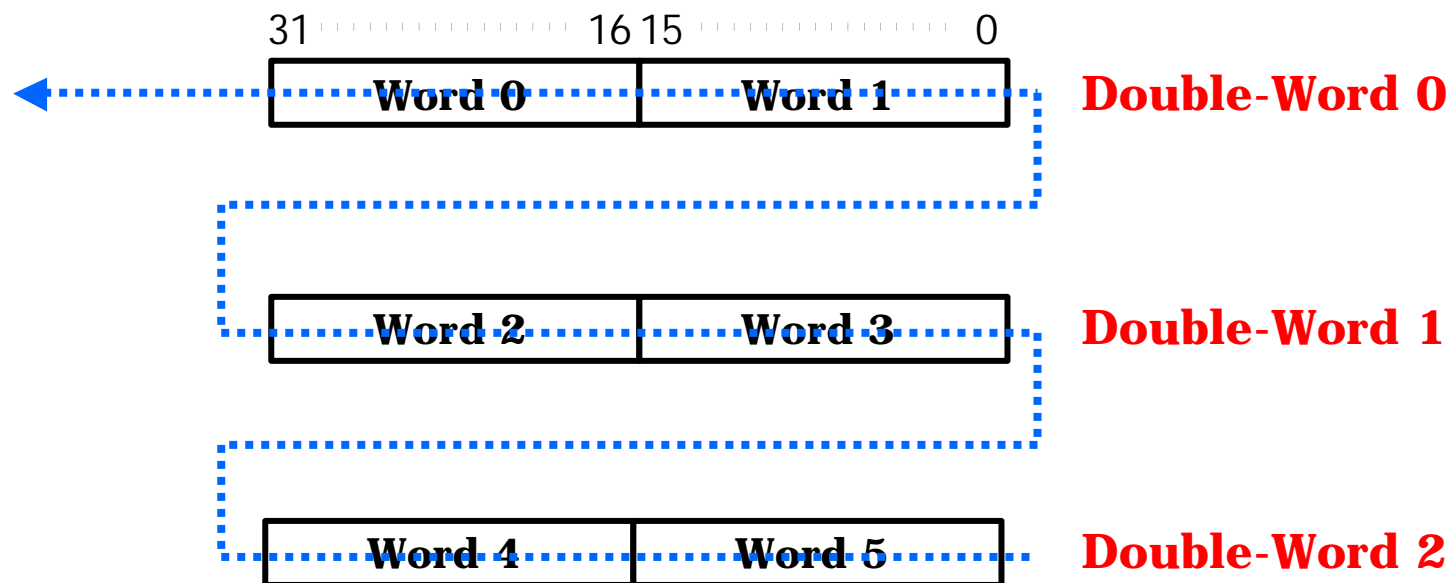
Byte ordering

MSB FIRST



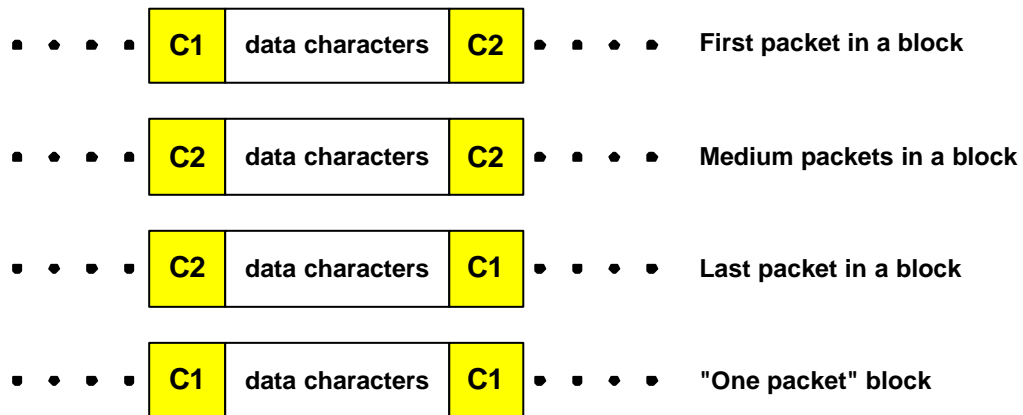
Byte ordering

MSB FIRST



Block Format

- The data are transmitted in variable length blocks.
- A block :
 - A sequence of packets.
 - Contain only data characters.
 - The CTRL chars are added in or taken out by the DAQ port.
- Four kinds of packet in a block :



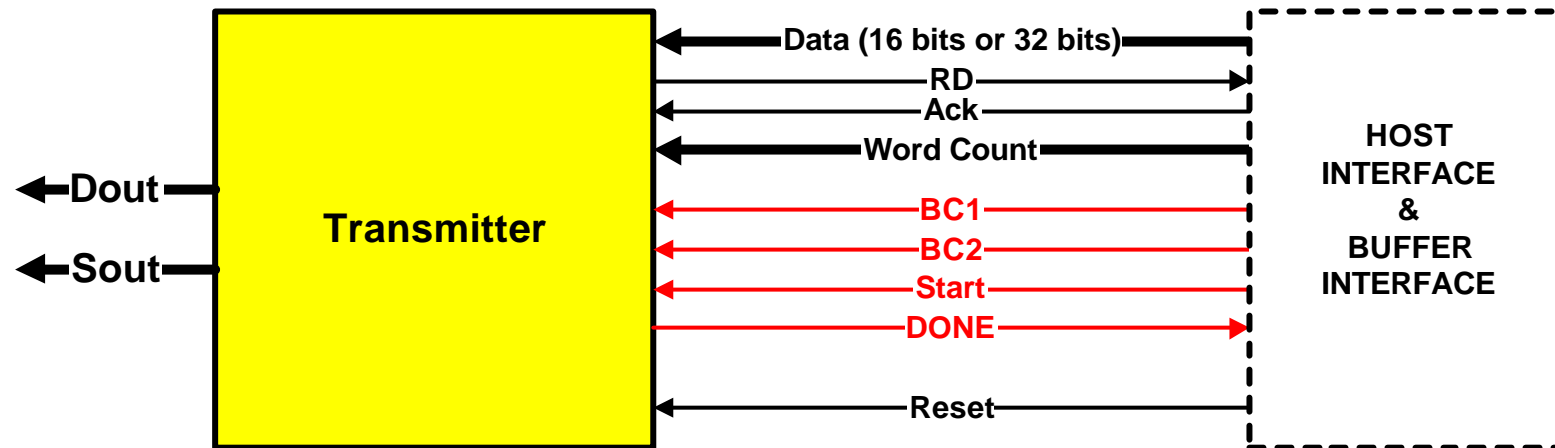


AMS DAQ Link Port

- A AMS DAQ port contains :
 - LVDS driver/receiver → individual IC
 - TX and RX → implemented in FPGA
 - Two buffers → individual IC (shared or dedicated)
 - Dual-port RAM or Single-port RAM
 - Size = Max packet

- System Clock = 100 MHz or 50 MHz

Transmitter (TX)



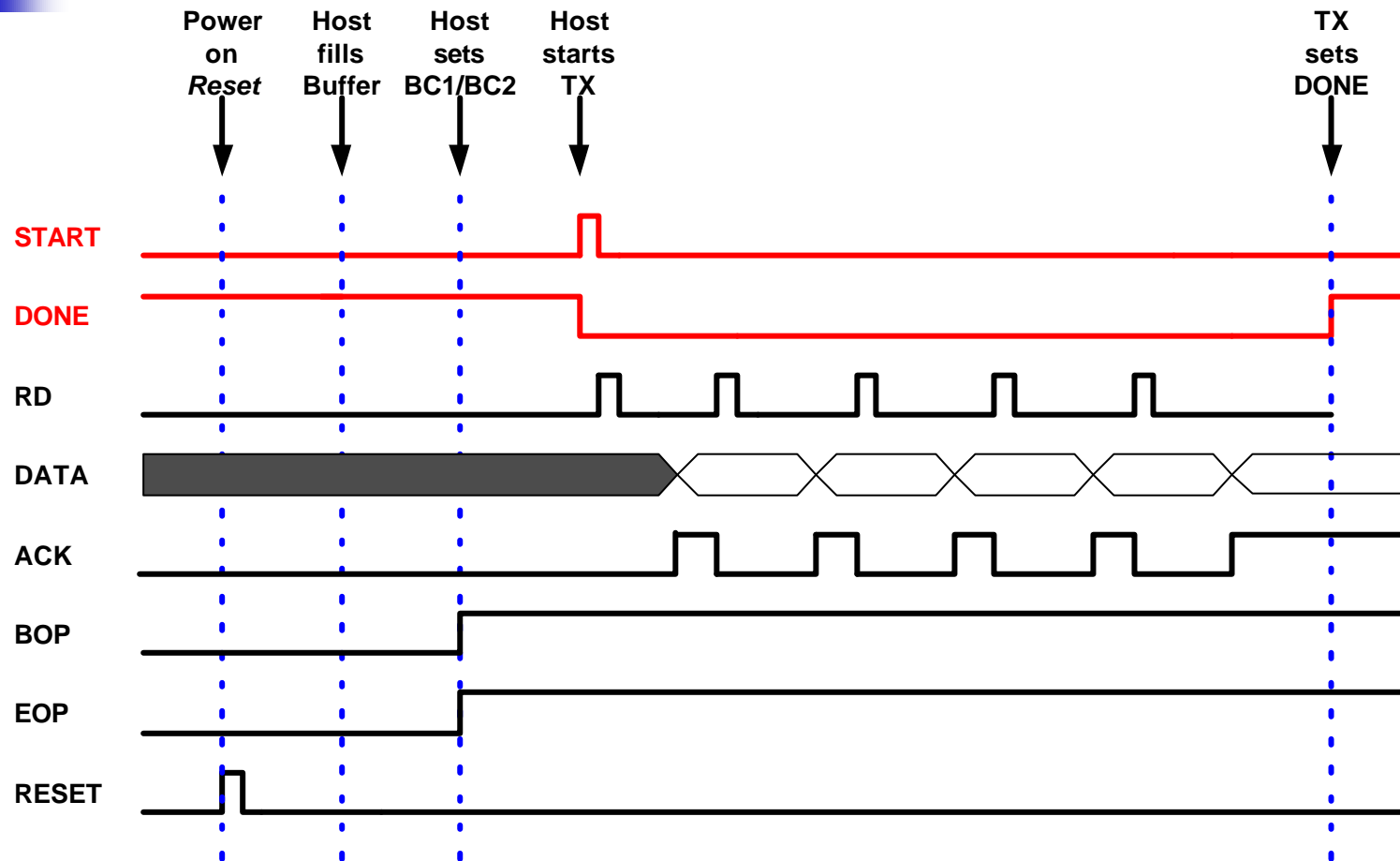
- ❑ TX is responsible for encoding and transmitting data using DS Encoding.
- ❑ The buffer and the host are not required to operate at 100 MHz.
 - ➔ TX provides the synchronization among them.
- ❑ If the buffer interface can't provide data on time,
 - ➔ Transfer NULL characters.



Signals for TX

- ❑ Data (I) : 16 bits or 32 bits, from the Host.
- ❑ RD (O) : Data Read signal.
- ❑ ACK(I) : Acknowledge for data read.
- ❑ WC (I) : The length of packet stored in buffer.
(The unit of WC is "WORD, 16bits".)
- ❑ Start (I) : Ask TX to send a packet stored in the buffer (Strobe-like).
- ❑ DONE : Inform the host the transmission is finished. TX is ready for the next packet.
- ❑ BC1, BC2 (I) : select which CTRL char shall be sent at beginning and end.
- ❑ RESET (I) : Reset signal for TX.

Relation Diagram - TX

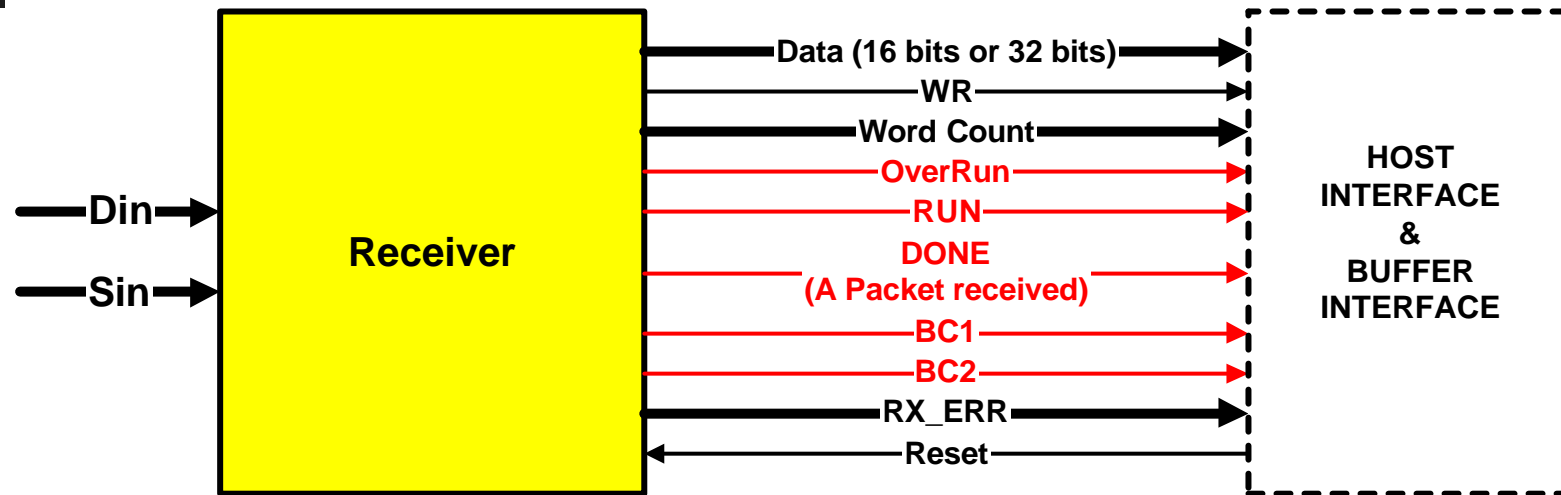




Requirements for RX

- ❑ To be ready for receiving packet after power on.
- ❑ Allow the Master to send a command when the host of slave does not work properly.
 - ➔ RX shall be able to decode few commands, like "BOOT" ...etc.

Receiver (RX)



- ❑ RX is responsible for decoding DS signals to produce characters.
- ❑ RX CLK is recovered by XORing the received D and S signals
 - ➔ $f = \text{half of data rate (50 MHz)}$
 - ➔ Both CLK edges are used to latch the incoming data.



Signals for RX

- ❑ Data (O) : 16 bits or 32 bits, to the Host.
 - ❑ WR (O) : Write Enable.
 - ❑ WC (O) : The length of packet stored in buffer.
(The unit of WC is "WORD, 16bits".)
 - ❑ DONE (O) : Inform the host that a packet is received and stored in the buffer.
 - ❑ RUN (O) : RX is receiving a packet.
 - ❑ OverRun (O) : The OverRun condition happens. (see later)
 - ❑ BC1, BC2 (O) : Show which kind of packet is received.
 - ❑ RX_ERR (O) : The receiver error are detected in the link. (see later)
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OverRun

□ OverRun :

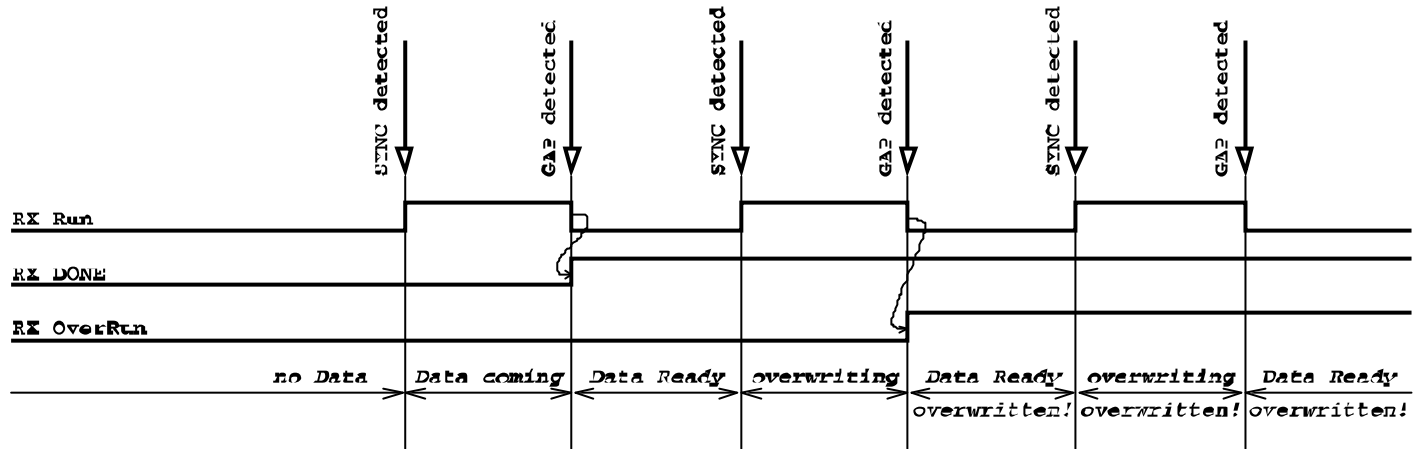
- RX receives a new packet, but the RX buffer is not ready.
- **Shall not happen in normal operation.**
- Rewrite buffer with "OverRun" packet.
 - ✓ Master shall realize that it's sending a "OverRun" packet.
 - ✓ Allow Master to store some data in RX buffer, which can be used as a booting parameter.

□ Two Conditions :

- The host isn't reading the RX buffer.
 - ✓ The OverRun signal is asserted.
- The host is reading the RX buffer.
 - ✓ The host shall check the RUN and DONE signals again at end of buffer reading.

RX Operation

AMS Wire: RX Operation



RX Status Register		
bits	when set ON	when set OFF
RX Run	SYNC detected	GAP detected
RX DONE	RX Run goes OFF	readout and RX Run is OFF
RX OverRun	RX Run goes OFF and RX Done is ON	readout and RX Run is OFF

bits			comments
OverRun	Done	Run	
0	0	0	no Data
0	0	1	Data coming
0	1	0	Data Ready
1	1	0	Data Ready (overwritten)
0	1	1	Data overwriting
1	1	1	Data overwriting
1	0	0	Impossible
1	0	1	Impossible

Δ.Ltdbedet 25/02/01 (mod.03/02/01. Mod by CH LIN 16/04/01)



RX Operation

- When does the host read the RX buffer ?
 - DONE=1 and RUN=0

- How to determine a successful RX buffer reading ?
 - Check the status register again at end of buffer reading.
 - DONE=0 and RUN=0



Receiver Errors

- Parity Error

- Packet Format Error :

- Missing BC1

- Missing BC2

- FCT (ESC) doesn't come with ESC (FCT).

- Packet length > buffer size



Revision History

- 10. 2000, Ver 1.0, First version
- 02. 2001, Ver 2.0 Changes
 - ➔ Change the data signal to 16 bits
 - ➔ Modify OverRun condition
 - ➔ WC added.
- 06. 2001, Ver 3.0 Changes
 - ➔ The data signal can be 16 bits (FE & CDDC) or 32 bits (MDC).
 - ➔ The bit and byte ordering is changed to "MSB first" (Big endian).
 - ➔ (BOP,EOP,OP_COMPL) are changed to (BC1,BC2,DONE)
 - ➔ TC is changed to "11110111" (x2 ESC) to have 2 more recovered RX CLKs at end.
 - ➔ The unit of WC is defined to be "WORD (16 Bits)".
 - ➔ Use A. Lebedev's proposal for the RX operation (normal & overrun conditions).