

# **Universal Slow Control Module**

## **USCM V01**

### **for AMS-II**

**Version 1.2**

**28 June 2000**

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III. Physikalisches Institut

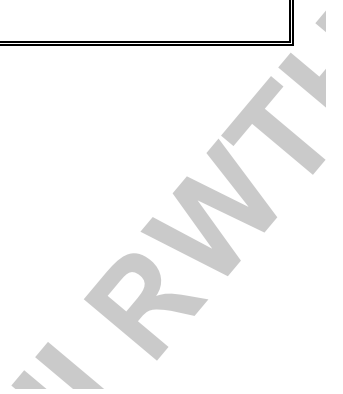
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## System Considerations

With the experience of the AMS-I slow control components as HCS, PCS, MSEA and MSEB modules we propose a more universal and flexible concept for a **Universal Slow Control Module (USCM<sup>4</sup>)**. This concept will reduce the number of different boards and so the costs. We'll be able to start the prototype production soon, which is necessary for software development. Based on a micro controller as the 8051 or upgraded versions it should be possible to fulfil the requirements in terms of computing power, speed and power consumption. We propose a module consisting of a basic part with double width EURO board dimensions and small application specific service modules, which will be connected to the basic board via a set of standardised miniature connectors with a partly fixed signal to pin allocation to the micro controller circuits, a second set of links to connectors. The basic board should consist of the micro controller, basic program memory (EPROM), EEROM for the program download section and a data memory (RAM), which is large enough for the foreseen applications and those one may consider. A standardised number of pins from the service module connectors should be provided to link I/O signals between a front- or rear panel to or from the service modules.

The service modules will contain electronic circuits for the DALLAS temperature sensors, high precision temperature sensors like PT100, circuits for B-field measurement, ADCs for voltage measurements, DACs for steering functions and digital I/O ports for simple control functions (power supply switching) .

## Latch Up Protection

The construction of small isles of functional groups with local supply current control circuits and an automatic shutdown plus recover in case of a fault should be sufficient to protect the electronic components. In case of the micro controller there should be an automatic reboot in case of a latch up induced power off cycle. All other circuits will be recovered be a more simple power off/on cycle without further actions.

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<sup>4</sup> This name may be changed at any time due to good arguments!

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## Communication

With the experience from AMS-I we propose the CAN bus as general communication link between the USCM and the MCCs. Two CAN bus controllers per USCM should be enough in terms on redundancy, because of the single redundancy of the micro controller circuit itself. The same type of CAN bus controller should be used by all AMS-II components in order to have the same performance in terms of address range, bus speed, protocol level (CAN 2.0B) etc. For debug purposes one or two RS232 port may be available.

## Component Selection & Layout

The component selection should be done under the aspect of thermal requirements, costs and pin pitch in terms of the possibility to fulfil the request for a MIL specs conformable board layout (wire and via dimensions). A selection of fine pitch components may reduce the space requirements of the semiconductors itself, but space needed to make all the connections to the associated circuits will consume all the space earned by the smaller components. In terms of costs it will not be possible to use MIL specified semiconductor components. Even under the aspect of board space requirements it will be necessary to omit MIL specified components, because these parts are mostly produced in the large 2.54mm pin spacing *dual in line* packages. The experience of AMS-I and other space missions gains that the semiconductor components of the industrial temperature range (-40 C +85 C) will fulfil the requirements of the control electronic.

## Connectors

An optional front panel will contain connectors for power – UPS or USCM switched – DALLAS sensor chain, analogue input and digital I/O. The same power input and signal I/O should be accessible at the (optional) rear connector. The USCM module will be operable in a test frame with spring forced connector needles connecting all relevant power and signal I/O lines. This method used for the board production of AMS-I slow control components allows the functional test without any strengthening of the space qualified connectors.

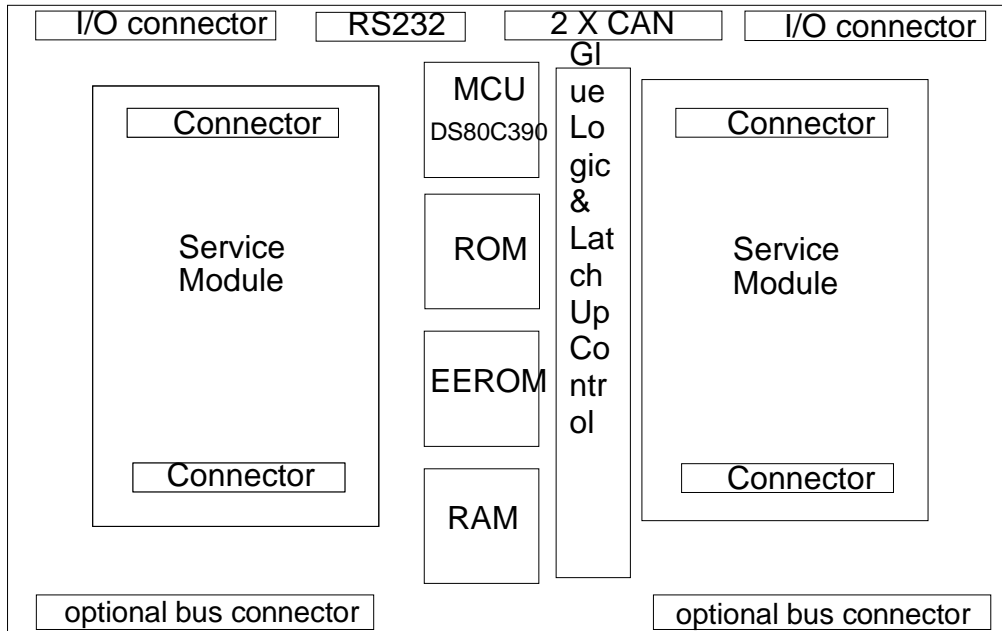
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# Universal Slow Control Module

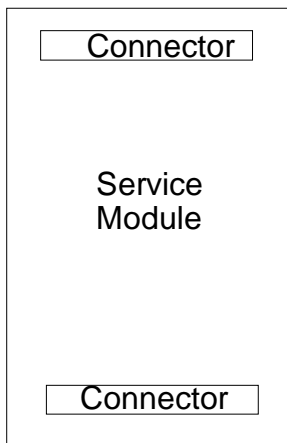
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23-05-2000

USCM-1



## Service Module Elements:



n x 8 channel 12 bit ADC

n x 8 channel 12 bit DAC

n x DS1820 port

n x PT100

n x digital I/O & special functions

local latch up control

## USCM Prototype

The prototype version of the USCM will be available October 2000. This version will run with the DS80C390 MCU chip at a basic crystal frequency at 14.74Mhz. The internal clock multiplier of the MCU gives 70% of the maximal clock speed. In case of higher clock frequencies we will need very fast memory components, which are partly not available and need additional power.

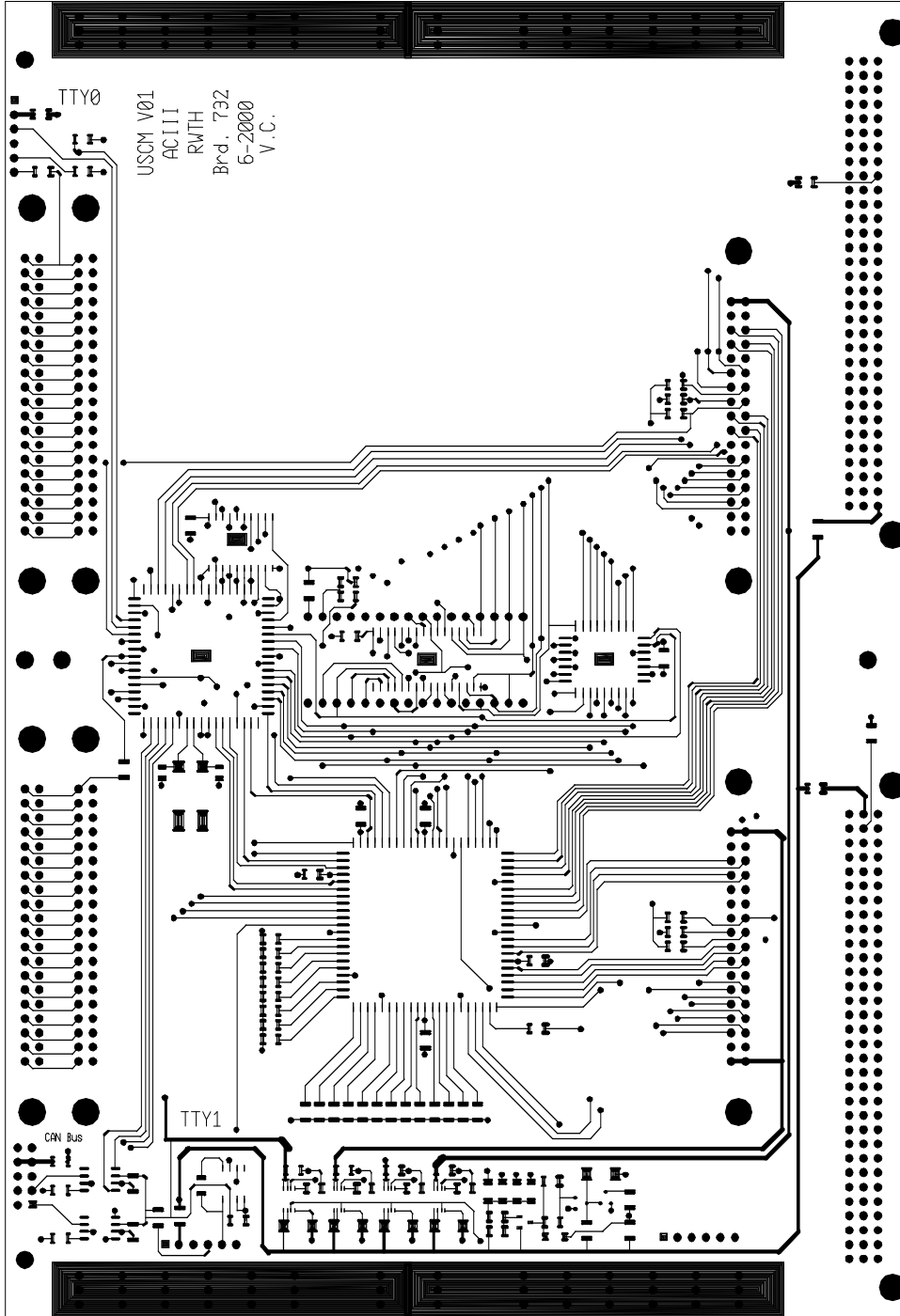
Beside the MCU three different memories are mounted on the main board. An EPROM (33kbyte, 70ns), a RAM (32kbyte, 45ns) and a EEROM (32kbyte, 70ns). For the prototype version all glue logic for port decoding will be done with one XILINX PLD. This PLD will only be used during the development phase, for the more final version the logic functions will be done with simple gate equivalents to reduce power and the risk of a latch up in a large device like a PLD.

Four different latch up protection circuits are provided, one for the MCU, one for the PLD and two for the **Service Modules** mounted on the main board.

The communication to the outside world may be done via two RS232 ports (TTL signals, the conditioning to RS232 standard has to be off board) and two CANbus ports (bus termination off board).

Two **Service Modules** of a dimension 125 mm X 75 mm are mounted on the main board (double Euroformat). Each SM has two connectors, one 34 pin connector for the link to the MCU signals to the board and a 40 pin connector for the I/O signals. The MCU data bus, 8 decoded port enable, 3 interrupt, 4 specific port pins from MCU are linked via the 34 pin connector. The board power of 5VDC is controlled by one latch up control circuit per SM.

For smaller application a version in single Euroformat will provide the space for one SM.



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**USCM Version 1**

**Memory Address Layout:**

Address Range	Module Type	Function	Size (kbyte)
0X00000 to 0X1FFFF	ROM	Boot & Program	128
0X20000 to 0X3FFFF	RAM	Data & Program	128
0X40000 to 0X5FFFF	EEROM	Data & Program	128
0X60000 to 0X6F000	2 Service Modules	16 I/O Ports	1

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## USCM Connectors

### RS232 Serial Ports

Connector/Pin	Signal	Connector/Pin	Signal
J2-1	GND	J1-1	GND
J2-2	1VCC <sup>Note</sup>	J1-2	2VCC <sup>Note</sup>
J2-3	TXD0	J1-3	TXD1
J2-4	RXD0	J1-4	RXD1
J2-5	MAN_RES	J1-5	MAN_RES
J2-6	GND	J1-6	GND

This pin allocation fits to the test clips of the AMS-I PCS, HCS, MSE modules.

Note: The 1VCC or 2VCC may be used to power the module (jumper selectable).

### CAN BUS I/O

Connector / Pin	Signal
J3-1	CAN_A-
J3-2	CAN_A+
J3-3	CAN_B
J3-4	CAN_B+
J3-5	NC
J3-6	NC
J3-7	3VCC <sup>Note</sup>
J3-8	3VCC <sup>Note</sup>
J3-9	GND
J3-10	GND

This pin allocation fits to the AMS-I test system for PCS, HCS and MSE modules.

Note: The 3VCC may be used to power the module (jumper selectable).

Two VME Bus type are provided to mount the USCM in a VME crate. The +5VDC (4VCC & 5VCC) and VME system ground may used to power the module (jumper selectable).

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## Service Module MCU Link Connectors

Connector/Pin	Signal	Connector/Pin	Signal
J9-1	VCC2	J10-1	VCC3
J9-2	VCC2	J10-2	VCC3
J9-3	GND	J10-3	GND
J9-4	GND	J10-4	GND
J9-5	AD0	J10-5	AD0
J9-6	AD1	J10-6	AD1
J9-7	AD2	J10-7	AD2
J9-8	AD3	J10-8	AD3
J9-9	AD4	J10-9	AD4
J9-10	AD5	J10-10	AD5
J9-11	AD6	J10-11	AD6
J9-12	AD7	J10-12	AD7
J9-13	Write_IO	J10-13	Write_IO
J9-14	Read_IO	J10-14	Read_IO
J9-15	CEIO_0	J10-15	CEIO_8
J9-16	CEIO_1	J10-16	CEIO_9
J9-17	CEIO_2	J10-17	CEIO_10
J9-18	CEIO_3	J10-18	CEIO_11
J9-19	INT0	J10-19	INT1
J9-20	INT2	J10-20	INT4
J9-21	INT3	J10-21	INT5
J9-22	RES_OUT	J10-22	RES_OUT
J9-23	TIM0	J10-23	TIM0
J9-24	TIM1	J10-24	TIM1
J9-25	T2	J10-25	T2
J9-26	T2EX	J10-26	T2EX
J9-27	CEIO_4	J10-27	CEIO_12
J9-28	CEIO_5	J10-28	CEIO_13
J9-29	CEIO_6	J10-29	CEIO_14
J9-30	CEIO_7	J10-30	CEIO_15
J9-31	GND	J10-31	GND
J9-32	GND	J10-32	GND
J9-33	VCC2	J10-33	VCC3
J9-34	VCC2	J10-34	VCC3

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**Service Module I/O Link Connectors**

SM-1

<b>Connector</b>	<b>Signal</b>	<b>Connector</b>
J6 Pins 1-40	I/O link	J5 Pins 1-40
Pin 40	Optional Ground	

SM-2

<b>Connector</b>	<b>Signal</b>	<b>Connector</b>
J7 Pins 1-40	I/O link	J8 Pins 1-40
Pin 40	Optional Ground	

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**Draft**

**Software Concept  
For The AMS II  
Universal Slow Control Module**

**Version 1.0**

**June 28 2000**

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## General

Based on our experience with the AMS I slow control HCS, PCS, MSEA, MSEB and TASE modules we intend to transfer our software concept to the Universal Slow Control Module<sup>9</sup> (**USCM**) being in development for AMS II.

Using the Dallas DS80C390 instead of the 87C51FA we'll gain a lot of performance because this processor executes instructions 3 times faster and has a built-in floating point unit. Although the software was written in assembler it should be easily transportable to the new platform since most of the platform dependent instruction sequences are already defined via macros.

## Monitor

The monitor will support up to four tasks as for AMS I, which seems to be sufficient. Due to the better processor performance the time slices foreseen for each task may be reduced in order to improve real time performance.

## Task 1

will be assigned to serial I/O for debug and software development.

## Task 2

will deal with the readout of ADCs, which may serve for different measurements (e.g. Pt100 temperature sensors, B-field sensors, currents, voltages), control DACs for e.g. current injection for B-field sensors and do digital I/O for e.g. control of power supplies, peripheral status information etc.

## Task 3

will handle the I/O via the two redundant CANbus ports.

## Task 4

is foreseen for the readout of the Dallas temperature sensors. We strictly recommend to use the 3-wire protocol (ground, data, Vcc).

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<sup>9</sup> V. Commichau, Universal Slow Control Module for AMS-II, Version 1.1, April 28 2000

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## Module Identification

As in AMS I there will be only one software version supporting all necessary combinations of Service Modules (SM). An unique identification number will be programmed into the USCM's ROM.

The signal conditioning will be done for the standard devices on the SMs. Identification of type and serial number of the service modules will done via an 8 bit SM identifier.

## CANbus addressing

Using the extended ( 29 bit ) identifiers there will be two address modes:

- a) LSB = 1 a *newborn* CANbus address is generated from the unique module identification number.
- b) LSB = 0 a *logical* CANbus address may be freely defined and stored into the EEPROM data section of the module.

The *logical* CANbus address will be used, if set in the EEPROM data section.

Whenever a defect module is to be replaced, software - program- and data sections - may be downloaded via CANbus ( *newborn* address ) into EEPROM with the system running. Data integrity is maintained by checksum.