

S-crate Physical Connections

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ABSTRACT

The AMS-02 detector electronics boards are distributed among different crates. The boards of the TOF and ACC systems are placed in the S-crates, with the only exception of the SFEC boards, which are installed inside the TOF detector. This paper describes the front-end electronics of the ACC and TOF subdetectors from the point of view of the physical connections on front panels and backplane.

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1. H ()

Changes since version 3.09 (Oct 23, 2006)

- Changed serigraphy on SFET2 and SFEA2 front panels (figure 1).

Changes since version 3.08 (Oct 13, 2006)

- Changed serigraphy on SDR2, SPT2, and SFEA2 front panels (figure 1).

Changes since version 3.02 (Mar 13, 2006)

- New SFET2 and SFEA2 design.
- Figure 1 updated.
- Backplane changed again.
- Added LVL1 lines on backplane.
- Changed SDR2 VME naming scheme.
- Dropped few tables.

Changes since version 2.35 (Dec 19, 2005)

- New SFET2 and SFEA2 design: front- and back- connections changed.
- Updated image of S-crate front-panels.

- Power lines to SFEC: ± 4.0 V (not 5.0 V) and 3.3 V.

Changes since version 2.33 (Dec 1, 2005)

- Fixed typos in the last two tables.

Changes since version 2.32 (Oct 25, 2005)

- SFEC power lines changed.

Changes since version 2.31 (Oct 17, 2005)

- SFEA2 VME connectors changed.

Changes since version 2.29 (Jun 29, 2005)

- ACC anodes come to SFEA2 via 50 Ohm coaxial cables.
- Changed SFEA2 front panel in figure 1.
- Changed SPT2 VME connectors and hence the backplane.
- No current monitor on the backplane.

Changes since version 2.26 (Mar 7, 2005)

- Added sketch of the AMS-02 crates (now figure 2).
- Changed SDR2 VME connectors.
- More complete description of SDR2 and SPT2 backplane connections.

Changes since version 2.15 (Aug 24, 2004)

- LeCroy output from SDR2 is now TTL3.3V instead of LVDS.
- Changed SDR2 VME pin-out.
- Changed SPT2 VME pin-out.
- Changed SFET2 VME pin-out.
- Named “SFEC 1” and “SFEC 2” the SPT2 front connectors (figure 1).
- Added tables 11 and 12.
- Updated figure 4.
- Dropped figures showing backplane lines and colors in VME pin-out tables.
- Added always powered LV lines for SFEC boards.

Changes since version 2.13 (May 24, 2004)

- Dropped table with board producers.
- Corrected tables in section 4.

Changes since version 2.12 (Apr 27, 2004)

- Changed FT distribution.
- Fix board/producer names

Changes since version 2.11 (Mar 26, 2004)

- Fixed SFEC-SPT2 twisted pair cable.

Changes since version 1.26 (Jul 28, 2003)

- S-crate drastically changed to optimize mass and power dissipation (Oct. 2003):
 - SHV has been moved outside the crate;

- SFET2 boards have now 4 input channels instead of 8, and use a single PCB. In addition there are 2 VME connectors instead of 1;
- SFEA2 is now on a single PCB, with 2 VME connectors;
- the two USCM disappeared (using the slots for the additional new SFET2 boards);
- the SFEC2 boards moved to the patch-panel on the detector;
- the SFEC boards are not redundant (hence, no “2” in the name), but
- dynodes charge is measured PMT-wise, whereas the anodes at the same counter side are still summed;
- SFEC boards communicate with SPT2; SPT2 sends dynode charges to SDR2 via TOFwire;
- SPT2 has 1 primary and 1 secondary VME connector (they were mixed hot+cold).

- Different kinds of link used for time and charge data.
- Tables 3, 4, 8, 9, 10 have been corrected;
- SFEC connectors were changed (table 6 and figure 4).

Changes since version 1.20 (Jul 2, 2003)

- Pin-out of rear connectors of FE boards has been changed.
- SFET2 boards have now the same orientation inside the crate.
- HOT/COLD pins changed into P/S (primary/secondary).
- Input voltage of boards has been adjusted.
- New names for front connectors. Added pin-out of front connectors.
- Fixed front connectors in SFEA2.

2. T AMS-02 S-

The AMS-02 detector electronics boards are distributed among different crates. The four “scintillators crates” or “S-crates” host the front-end boards of the time of flight (TOF) and anticoincidence (ACC) systems, with the exception of the SFEC boards (which measure the charge given by the TOF dynodes), installed inside the TOF detector. In addition, each crate hosts the “pre-trigger” logics preceding the trigger boxes JLV1A and JLV1B.

Each S-crate serves two TOF half-planes and four ACC photomultiplier tubes (PMT). The only difference between upper and lower S-crates is the number of TOF channels: the upper TOF planes (S1 and S2) have 8 paddles each, while the lower TOF planes have 10 (S3) and 8 (S4) scintillators. The two outermost counters in each plane have a different shape from the others. These counters have 3 PMTs per side on planes S1 and S4; 4 PMTs per side in planes S2 and S3.

Each S-crate (figure 1) contains the same number and type of boards: one scintillator data reduction redundant unit called SDR2, four scintillator front-end TOF redundant boards called SFET2, one scintillator front-end ACC redundant board called SFEA2, one redundant scintillator pre-trigger board (SPT2). Table 1 shows the analog inputs of all the front-end (FE) boards (see ref. [1] for the details of the detector cabling).

The high-voltage (HV) lines that feed the TOF and ACC phototubes come from a redundant module called SHV (scintillators high-voltage brick), placed outside the S-crate. The low-voltage (LV) lines feeding a given S-crate come from DC/DC converters placed in the four “tracker & scintillator power distribution” (TSPD) crates. These converters are fed by 2 independent input 28 V_{cc} lines, each powering half of the S-crate boards.

For ACC and TOF electronics, redundancy means that there are two identical copies of the each functional unit¹ (SDR, SFET, SFEA, SPT, LV and HV) and at any time only one is turned on (“hot” state). The other unit (the “cold” one) is not powered until it is necessary to recover a possible hardware problem of the first one. To enforce the redundancy, there is no cross connection between the two halves of the S-crate, of the HV brick and of the DC/DC converters, neither on the powering side, nor on the communication side². Usually, only one of these 28 V_{cc} lines is turned on, determining what is the hot half of the S-crate.

The communication between boards within the S-crate is done via a backplane, which is also used to bring the power from the DC/DC converters to the boards. Powering cables from DC/DC converters are to be screwed to the backplane. Front connectors are used for the communications with the external world (figure 1).

¹With the exception of SFEC boards, not redundant.

²Apart from SFEC LVDS and LV lines on SPT2.

Board	TOF		ACC
	anodes	dynodes	anodes
SFEA2	0	0	4
SFET2	5	0	0
SFEC	0	20	0

Table 1. Analog input lines of the front-end boards.

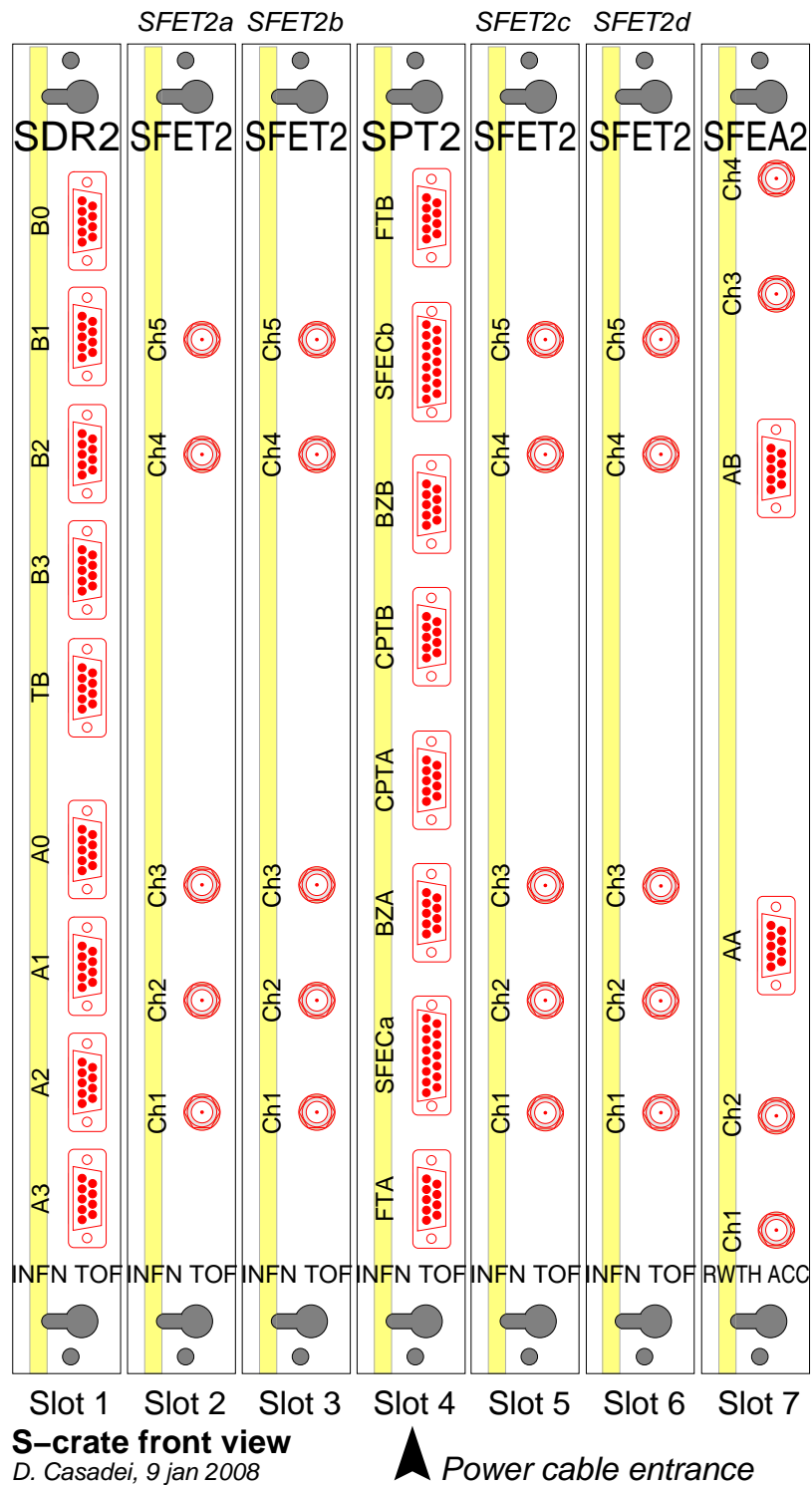


Figure 1. Sketch of the S-crate front view. Front connectors are in red, PCBs in yellow. SFECs are placed on the detector and are connected to the SPT2 front panel via 15-pins connectors (labelled SFECa and SFECb).

2.1. Front-end electronics

The front-end modules are on the SFEx2 boards (each board containing two SFEx modules, hot+cold). Data from SFEx are collected by the corresponding SDR module through the internal links and then transmitted to the higher hierarchy level (4 JINJ boards) through the AMSwire serial links [2].

Time data are sent via a serial link named “TOFwire”, that is also used to send commands from SDR to SFEx. Charge data are read in a different way, using a common strobe sent by SDR [3].

The TOFwire serial protocol is a simpler subset of the AMSwire protocol, and will be described in a separate document [3]. Here the only important feature of AMSwire and TOFwire is the cabling: one AMSwire (TOFwire) link requires 4 LVDS (TTL) lines.

Each SDR module³ is serially connected (via backplane, TOFwire protocol) to the corresponding SFEx modules and to the corresponding SPT module⁴, i.e. to the modules powered by the same 28 V_{cc} line. In addition, each SDR is connected (via LVDS cables, AMSwire serial protocol) to the four JINJ boards (each JINJ is connected to both hot and cold SDR modules) and (via LVDS lines, LeCroy bus protocol) to the SHV.

The SFET module receives 5 negative analog inputs (TOF anodes). The anode signal is split into two different paths. The smaller signal is used to measure the charge, the higher one is used to give the fast trigger and to measure the particle crossing time. The details of the SFET working scheme are given in a separate document [4].

The SFEA module is a simpler version of the SFET, which is adapted to the ACC signal. The details are given in a separate document [4].

In addition to ACC and TOF anode charge measurement, the TOF dynode charge is also measured by the SFEC redundant board. The details are given in a separate document [4].

The logic signals needed by the SPT2 correspond to singly charged particle signals (TOF anode passing the “high threshold” HT on SFET/SFEA modules) and to “ $Z \geq 2$ ” signals (anode passing the “super high threshold” SHT). Logic signals coming from each (half) TOF plane connected to a given S-crate are logically OR’ed⁵ in order to send to JLV1x only one LVDS line per signal per half TOF plane. These combined signals are called “charged particle” (CP,*n* with *n* = 0 . . . 7— signals above the HT), “charged particle in the center” (CT,*n* — signals above the HT in central TOF counters), “big Z” (BZ,*n* — signals above SHT) [5].

In addition, SPT2 receives the 4 + 4 LVDS FT signals coming from the JLV1x, forwarded to the SFET2 boards via backplane. The details of the pre-trigger logics can be found in a separate document [6].

The TOF dynode charge is measured on the detector by the 2 SFEC boards (one on each patch-panel). The SDR module sends the sample-and-hold signal and the strobes via TTL3.3V to LVDS drivers placed on SPT2, as described in [3], where hot and cold TTL lines are summed together before being converted into LVDS signals.

The SFEC modules send back to SPT2 the ADC words via LVDS data+strobe lines, converted on SPT2 into hot+cold TTL3.3V lines that reach SDR2 via the backplane [3].

³One SDR module is half of the SDR2 board.

⁴One SFEx module is half of the SFEx2 board; one SPT module is half of the SPT2 board.

⁵Signals sent to JLV1A and JLV1B are active low, hence the logical sum is electrically an AND operation.

2.2. Slow control

There are no USCM boards [8] in the S-crate. Temperatures of crates and detectors are read by external USCM boards. Temperatures of SFET2 and SFEA2 are read by the boards themselves and are collected by SDR2 [3].

The HV settings are transmitted to the SHV by the SDR2 via LVDS lines (LeCroy bus). LeCroy wires will be soldered on the backplane and will have a flying connector.

The status of each board is controlled by SDR2. The control of the thresholds on analog signals is done by SDR2 too [3].

2.3. Powering

The S-crate is powered by the tracker and scintillator power distributor (TSPD) boxes [7], that contains the DC/DC converters needed to feed the boards with the different lines as showed in table 2.

SFEC boards receive LV lines from SPT2, where primary and cold lines are summed together.

The TOF and ACC primary tubes powering is the task of the redundant HV brick. For each half brick (connected to a separate $28 V_{cc}$ input line) the high voltage elevator (HVE) DC/DC converter gives up to $-2500 V_{cc}$ to the different linear regulators (LR). The LRs have a default reference value of $-1950 V$ and can be tuned by the SHV controller with a 8-bit DAC from $-2300 V_{cc}$ to $-1400 V_{cc}$ (min. step $3.5 V$).

3. E

All external connections are on the front panels of the S-crate boards (see figure 1) but powering and LeCroy link, which are located in the backplane. Figure 2 shows the placement on the AMS-02 radiator walls of the S-crates, the SHVs and the DC/DC converter boxes (TSPDs). Red lines represent low voltage, whereas dark-green lines are LeCroy connections.

Board	Slot	+28V _{cc}	+3.3V _{cc}	+5.1V _{cc}	±5.6V _{cc}
SHV	—	y	y	y	n
SFEC	—	n	n	y*	y*
SFEC	—	n	n	y*	y*
SDR2	1	n	y	n	n
SFET2	2	n	y	y	y
SFET2	3	n	y	y	y
SPT2	4	n	y	y	y
SFET2	5	n	y	y	y
SFET2	6	n	y	y	y
SFEA2	7	n	y	y	y

Table 2. Low voltage connections for the ACC & TOF electronics. SFEC needs +3.3 V for the digital part (originating from the 5.1 V backplane line, via SPT2), +3.0 V and $-2 V$ for the analog part. The lines for the analog part are produced on the SPT2 starting from the $\pm 5.6 V$ lines, which become $\pm 4.0 V$ and are adjusted to the final values on board of the SFEC.

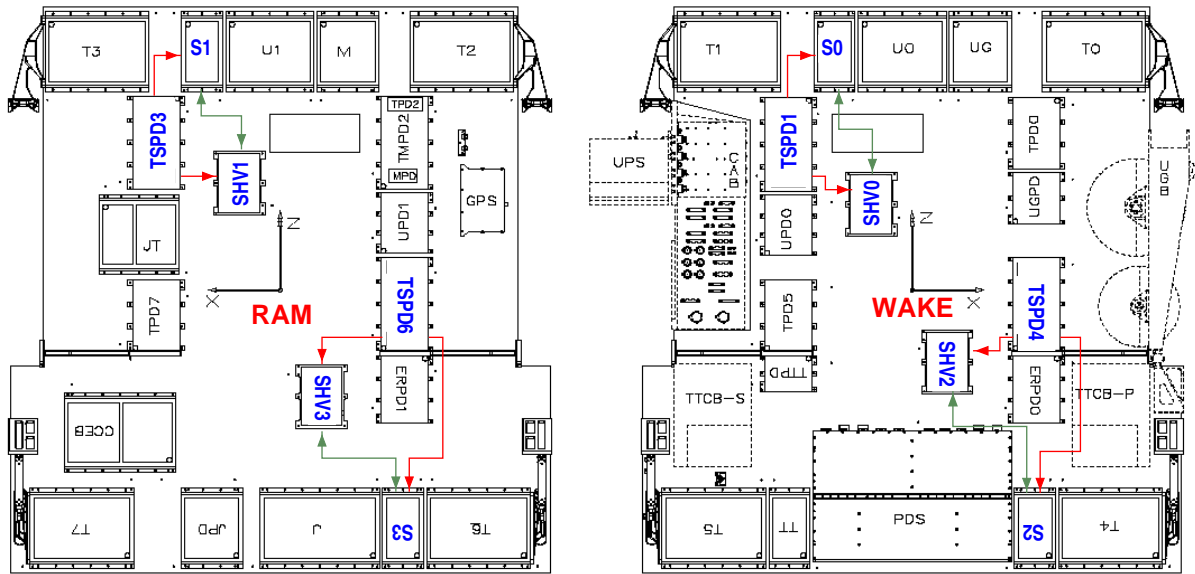


Figure 2. AMS-02 electronics crates (“ram” side on the left, “wake” side on the right). S-crates are labelled “S0” ... “S3”. Green lines represent control links, whereas red ones are power lines.

3.1. SDR2

Each SDR2 consists of two identical SDR modules, physically mounted on the same PCB. Each SDR2 has 2×4 μ D 9-pins connectors (see §A.1) dedicated to the AMSwire links with the four JINJ (connectors named “AWP1” ... “AWS4” in figure 1). In addition, one μ D 9-pins connector is used to receive the two LV1 signals from JLV1A and JLV1B, and to send them the two BUSY signals corresponding to the two SDR modules. All signals received/transmitted with the front panel connectors are LVDS differential signal on twisted pairs, active low [5].

3.2. SFET2

Each SFET2 consists of two identical SFET modules, and has 5 coaxial input connectors for TOF anodes.

3.3. SFEA2

Each SFEA2 consists of two identical SFEA modules. The SFEA2 receives 4 anode signals from ACC. In addition it sends logical signals corresponding to singly charged particles to the two JLV1x.

The front panel of the SFEA2 has 4 coaxial input connectors and two μ D 9-pins connectors for the output LVDS signals sent to JLV1A and JLV1B (see §A.2).

3.4. SFEC

The front panel of the SFEC has one μ D 15-pins connector (see §A.3) with the LV and LVDS digital lines.

3.5. SPT2

The SPT2 front panel has six μ D 9-pins connectors: 2 are used to send CP,n and CT,n to JLV1A and JLV1B; 2 are used to send BZ,n to JLV1A and JLV1B; 2 are used to receive the 4 + 4 LVDS FT signals from JLV1A and JLV1B.

In addition, the SPT2 hosts the two μ D 15-pins connectors used to communicate with the SFEC boards (see §A.3).

3.6. HV brick

The HV brick consists of the SHV and its controller SHVC. The SHV is doubly redundant, and is formed by one redundant HVE and three “drawers” containing 8 redundant LR each. SHVC is doubly redundant too. The HV settings are controlled by the SDR2 board via 2 (primary+cold) LeCroy links.

4. I

All internal connections are on the rear part of the S-crate boards, via the backplane. All boards have two 96-pins VME connectors (apart from SFECs, which are not inside the S-crate), whose pin assignments can be found in appendix B.

Digital signals transmitted by the backplane follow the TTL 3.3 V standard. Each board can be switched off by SDR2 using the status control lines (“on/off control”), which are doubled for redundancy.

4.1. SDR2

Two 96-pins VME connectors (1 primary, 1 secondary, see tables 14 and 13 in appendix B), each with:

No.	Connection type	used pins	No.	Connection type	used pins
6	TOFWire TTL links	24	7	charge strobes	6
9	charge inputs	18	1	LeCroy bus	4
7	status monitor lines	7	7	on/off control	7
1	TTL FT	2	3	+3.4 V _{cc} (line + return)	6
2	Chassis GND	2	1	current monitor (<i>not used</i>)	3
2	LVL1 outputs	2	6	spare	6
—	Grounding	9			

The 6 primary TOFWire links connect the primary SDR module with: the 4 primary SFET modules, the primary SFEA module, and the primary SPT module. The 7 primary charge strobes go to: the 4 SFET modules, the SFEA module, the 2 SFECs. The 9 input charge links come from: the 4 SFET modules, the SFEA module, and the SFECs (two data lines per SFEC). All SFET2s and the sfea2 are connected to the 2 level-1 trigger lines.

The SDR module checks and controls the status of the SPT module and of each FE module. Idem for secondary parts (on the other connector).

4.2. SFET2

Two 96-pins VME connectors (1 primary, 1 secondary, see tables 18 and 17 in appendix B), each one with:

No.	Connection type	used pins	No.	Connection type	used pins
1	TOFwire TTL link	4	1	charge strobe	1
1	charge output	2	1	on/off control	2
1	status monitor	1	1	FT in	2
5	HT TTL out	5	5	SHT TTL out	5
3	+3.3 V _{cc}	4	3	+5.6 V _{cc}	4
3	-5.6 V _{cc}	4	2	LVL1 in	2
—	Grounding	60			

4.3. SFEA2

Two 96-pins VME connectors (1 primary, 1 secondary, see tables 20 and 19 in appendix B), each one with:

No.	Connection type	used pins	No.	Connection type	used pins
1	TOFwire TTL link	4	1	charge strobe	1
1	charge output	2	1	on/off control	2
1	status monitor	1	1	FT TTL in	2
3	+3.3 V _{cc}	3	3	+5.6 V _{cc}	3
3	-5.6 V _{cc}	3	10	floating	10
2	LVL1 in	2	—	Grounding	63

4.4. SPT2

Two 96-pins VME connectors (1 primary, 1 secondary, see tables 16 and 15 in appendix B), each one with:

No.	Connection type	used pins	No.	Connection type	used pins
1	TOFwire TTL link	4	1	charge strobes	2
2	charge output	8	2	on/off control	4
2	status monitor	2	6	LVDS FT out	12
18	HT TTL in	18	18	SHT TTL in	18
3	+3.3 V _{cc} (line + return)	6	2	+5.6 V _{cc}	2
2	return	2	2	-5.6 V _{cc}	2
2	Chassis GND	2	—	Grounding	14

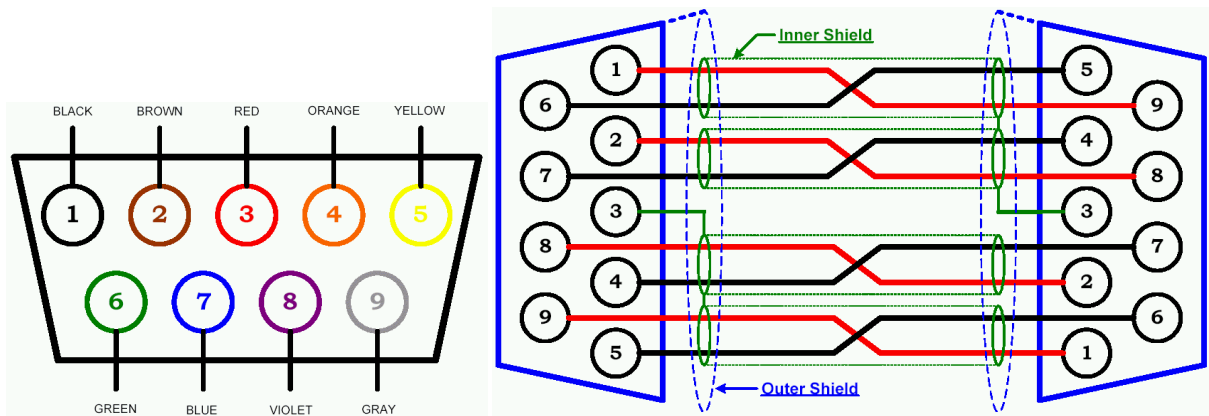


Figure 3. Pin-out in front of the plug (left) and cabling (right) of the μ D 9-pins connectors [5].

A. F

Figure 3 shows a sketch of the μ D 9-pins connectors pin-out and cabling.

NB. The signal names in the subsections below carry no information about the crate identity.

A.1. SDR2

SDR2 has nine μ D 9-pins front connectors. The central connector carries the two input LV1 signals, named LV1A and LV1B, and the two output busy signals, called BUSYA and BUSYB [5], as reported in table 3.

Pin	Signal name	Pin	Signal name	Pin	Signal name
1	LV1B-P	2	LV1A-P	3	GND
4	BUSYB-N	5	BUSYA-N	6	LV1B-N
7	LV1A-N	8	BUSYB-P	9	BUSYA-P

Table 3. SDR2: central connector (BL1) pin-out.

SDR2 has four AMSwire identical connectors for each SDR module, called AWP_x (primary) and AWS_x (secondary). The connector pin out is reported in table 4 [9].

Pin	Signal name	Pin	Signal name	Pin	Signal name
1	Din+	2	Sin+	3	Inner Shield
4	Sout-	5	Dout-	6	Din-
7	Sin-	8	Sout+	9	Dout+

Table 4. SDR2: AMSwire connectors (AWP_x , AWS_x) pin-out.

A.2. SFEA2

SFEA2 has 4 coaxial 50 Ohm input connectors, and two μ D 9-pins output connectors (named VTP and VTS) for ACC veto signals sent to the trigger boxes (JLV1A, JLV1B). Table 5 shows the veto

connectors pin-out (adapted from [5]).

Pin	Signal name	Pin	Signal name	Pin	Signal name
1	ACC-3-P	2	ACC-2-P	3	GND
4	ACC-1-N	5	ACC-0-N	6	ACC-3-N
7	ACC-2-N	8	ACC-1-P	9	ACC-0-P

Table 5. SFEA2: output veto connectors (VTP, VTS) pin-out.

A.3. SFEC

Each SFEC has one μ D 15-pins input connector. The pin-out is shown in table 6 and figure 4.

Pin	Signal name	Pin	Signal name	Pin	Signal name
1	+3.3 V	2	-4.0 V	3	Clock ₋
4	D2 ₋	5	D2 ₊	6	S2 ₋
7	S1 ₊	8	D1 ₋	9	+4.0 V
10	Ground	11	Clock ₊	12	Ground
13	S2 ₊	14	S1 ₋	15	D1 ₊

Table 6. SFEC 15-pins connector pin-out. D1 and S1, D2 and S2, are the data+strobe digital lines used to send bits to SDR2. SDR2 sends fast trigger, sample&hold, and clocks on the Clock line.

A.4. SPT2

SPT2 has six μ D 9-pins and two μ D 15-pins front connectors (see figure 1). The pin-out of the latter ones is reported in table 7.

Pin	Signal name	Pin	Signal name	Pin	Signal name
1	D1 ₊	2	S1 ₋	3	S2 ₊
4	D2 ₋	5	D2 ₊	6	Clock ₊
7	Ground	8	+4.0 V	9	D1 ₋
10	S1 ₊	11	S2 ₋	12	Ground
13	Clock ₋	14	-4.0 V	15	+3.3 V

Table 7. SPT2 15-pins connector pin-out. D1 and S1, D2 and S2, are the data+strobe digital lines used to send bits to SDR2. SDR2 sends fast trigger, sample&hold, and clocks on the Clock line.

Connectors FTA and FTB receive four LVDS FT signals each, coming from JLV1A and JLV1B respectively, whereas connectors CPTP and BZP (primary) or CPTS and BZS (secondary) send CP, CT, BZ signals to *both* JLV1A and JLV1B. Tables 8, 9 and 10 (adapted from [5]) show the pin-out of these connectors.

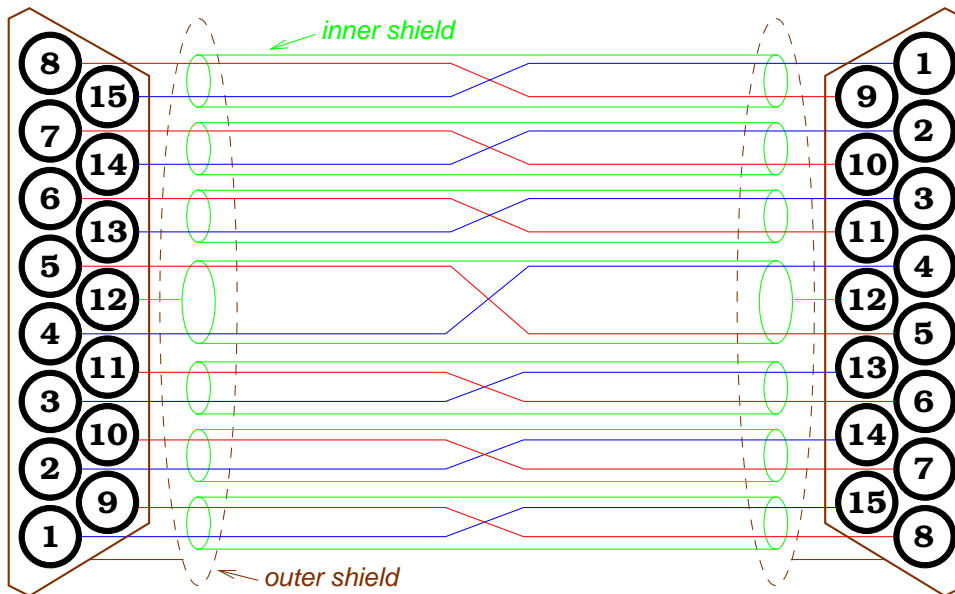


Figure 4. Pin-out in front of the plugs of the SFEC-SPT2 15-pins twisted cable.

Pin	Signal name	Pin	Signal name	Pin	Signal name
1	FT-3-P	2	FT-2-P	3	GND
4	FT-1-N	5	FT-0-N	6	FT-3-N
7	FT-2-N	8	FT-1-P	9	FT-0-P

Table 8. SPT2: input FT connectors (FTA, FTB) pin-out.

Pin	Signal name	Pin	Signal name	Pin	Signal name
1	CT-1-P	2	CT-0-P	3	GND
4	CP-1-N	5	CP-0-N	6	CT-1-N
7	CT-0-N	8	CP-1-P	9	CP-0-P

Table 9. SPT2: output CP, CT connectors (CPTP, CPTS) pin-out.

Pin	Signal name	Pin	Signal name	Pin	Signal name
1	Floating	2	Floating	3	GND
4	BZ-1-N	5	BZ-0-N	6	Floating
7	Floating	8	BZ-1-P	9	BZ-0-P

Table 10. SPT2: output BZ connectors (BZP, BZS) pin-out. Pins 1, 2, 6, 7 are floating to avoid ground loops.

B. B

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B.1. Legenda

Here we explain the symbols appearing in the following tables. Below, it is always $h = \text{S/P}$ (secondary/primary), whereas D = data, E = enable, S = strobe, I = input, O = output.

+3V3 <i>h</i>	input +3.3 V line
+5V1 <i>h</i>	input +5.1 V line
+5V6 <i>h</i>	input +5.6 V line
-5V6 <i>h</i>	input -5.6 V line
CHASGND	chassis ground;
CS <i>n</i> <i>h</i>	charge strobe, $n = 1..7$;
CTRL <i>h</i> <i>n</i>	control line, $n = 1..6$;
CW <i>n</i> <i>t</i> <i>h</i>	charge link (3 pins), $n = 1..9$ and $t = \text{D, S}$;
FT <i>st</i>	fast trigger (TTL), $st = \text{PJ, PK, SL, SM}$;
GND	grounded line;
HT <i>n</i> <i>h</i>	high threshold (TTL), $n = 1..18$
IMON <i>h</i> <i>t</i>	current monitor, $t = \text{E, D, S}$ (<i>not used</i>);
MON <i>h</i> <i>n</i>	monitor line, $n = 1..6$;
R <i>h</i> <i>n</i>	reserved (spare pin), $n = 1..9$;
RET <i>x</i> <i>h</i>	return line of power supply, $x = 3, 5$;
SHT <i>n</i> <i>h</i>	super high threshold (TTL), $n = 1..18$
TW <i>h</i> <i>n</i> <i>t</i> <i>v</i>	TOFwire link (4 pins), $n = 1..6$, $t = \text{D, S}$ and $v = \text{I, O}$;

NB. On each board, in the primary half the two FT signals (PJ, PK) must be combined (logical OR); in the secondary side the two FT signals (SL, SM) must be combined.

B.2. SDR2

Tables 13 and 14 show the pin-out of the SDR2 backplane VME connectors. The SFEC boards are not redundant: they receive power lines dioded inside SPT2 and send back to SPT2 unique charge LVDS links (data/strobe), converted into two TTL links connected to both halves of the SDR2 board. Each SFEC has two measurement units and two charge links, but receive only one strobe sequence from SDR2 [3]. No monitor/control is foreseen for SFECs.

B.3. SPT2

Tables 11 and 12 show the correspondence between SPT2 backplane (tables 15 and 16) and front connector lines, on the μD 15-pins connectors used to communicate with the two SFEC boards (tables 7 and 6). The analog LV lines (+3.0 V and -2.0 V) are obtained on SPT2 from the ± 5.6 V lines. Both primary and secondary lines are joined before going to the two SFEC boards.

— LVDS —		SFEC 1 pin	Direction SPT2 ↔ SFEC	— TTL —
SPT2 15-pin conn. Pin	Sign. name			Backplane, secondary
1	D1+	15	←	CW6D
2	S1-	14	←	CW6S
3	S2+	13	←	CW7S
4	D2-	4	←	CW7D
5	D2+	5	←	CW7D
6	Clock+	11	→	CS6
7	Ground	10		
8	+3.0 V	9	→	
9	D1-	8	←	CW6D
10	S1+	7	←	CW6S
11	S2-	6	←	CW7S
12	Ground	12		
13	Clock-	3	→	CS6
14	-2.0 V	2	→	
15	+3.3 V	1	→	

Table 11. Correspondence between backplane and front connector lines, for SFEC 1.

— LVDS —		SFEC 2 pin	Direction SPT2 ↔ SFEC	— TTL —
SPT2 15-pin conn. Pin	Sign. name			Backplane, primary
1	D1+	15	←	CW8D
2	S1-	14	←	CW8S
3	S2+	13	←	CW9S
4	D2-	4	←	CW9D
5	D2+	5	←	CW9D
6	Clock+	11	→	CS7
7	Ground	10		
8	+3.0 V	9	→	
9	D1-	8	←	CW8D
10	S1+	7	←	CW8S
11	S2-	6	←	CW9S
12	Ground	12		
13	Clock-	3	→	CS7
14	-2.0 V	2	→	
15	+3.3 V	1	→	

Table 12. Correspondence between backplane and front connector lines, for SFEC 2.

Other board pin	SDR2 pin/signal		Other board pin	SDR2 pin/signal		Other board pin	SDR2 pin/signal				
SFEA2	A5	A1	TWP5DO	SFEA2	A4	B1	TWP5SI	SFEA2	A3	C1	TWP5DI
SFEA2	A6	A2	TWP5SO	SFET2d	A4	B2	TWP4SI	SFET2d	A3	C2	TWP4DI
SFET2d	A5	A3	TWP4DO	SFET2c	A4	B3	TWP3SI	SFET2c	A3	C3	TWP3DI
SFET2d	A6	A4	TWP4SO	SFET2a	A4	B4	TWP1SI	SFET2a	A3	C4	TWP1DI
SFET2c	A5	A5	TWP3DO	SFET2b	A4	B5	TWP2SI	SFET2b	A3	C5	TWP2DI
SFET2c	A6	A6	TWP3SO	SPT2	A6	B6	TWP6SI	SPT2	A5	C6	TWP6DI
SFET2a	A5	A7	TWP1DO			B7	GND			C7	GND
SFET2a	A6	A8	TWP1SO			B8	GND			C8	GND
		A9	GND	SFET2b	A6	B9	TWP2SO	SFET2b	A5	C9	TWP2DO
SFEA2	A29	A10	CSP1	SPT2	A8	B10	TWP6SO	SPT2	A7	C10	TWP6DO
		A11	spare	SFET2d	A29	B11	CSP4	SFET2c	A29	C11	CSP3
SPT2	B10	A12	CSP6	SFET2a	A29	B12	CSP1	SFET2b	A29	C12	CSP2
		A13	GND	VME sec.	B13	B13	CWP7S	VME sec.	C13	C13	CWP7D
SFET2a	A2	A14	CTRLP1	VME sec.	B14	B14	CWP7S	VME sec.	C14	C14	CWP7D
		A15	spare	SPT2	B14	B15	CWP6S	SPT2	B12	C15	CWP6D
SFET2b	A2	A16	CTRLP2	SPT2	B18	B16	CWP6S	SPT2	B16	C16	CWP6D
		A17	spare	SFEA2	A31	B17	CWP5S	SFEA2	A30	C17	CWP5D
SPT2	A2	A18	CTRLP6	SFET2d	A31	B18	CWP4S	SFET2d	A30	C18	CWP4D
		A19	spare	SFET2c	A31	B19	CWP3S	SFET2c	A30	C19	CWP3D
SPT2	C2	A20	CTRLP7	SFET2b	A31	B20	CWP2S	SFET2b	A30	C20	CWP2D
		A21	spare	SFET2a	A31	B21	CWP1S	SFET2a	A30	C21	CWP1D
		A22	spare	SFET2c	A2	B22	CTRLP3	SPT2	C3	C22	MONP7
SFEA2	A2	A23	CTRLP5	SFET2d	A2	B23	CTRLP4	SPT2	A3	C23	MONP6
SFE*	A10	A24	LV1PA	SFE*	A9	B24	LV1PB	SFEA2	A32	C24	MONP5
S9074 gnd		A25	RET3P	S9074 gnd		B25	RET3P	Imon		C25	IMONPD
		A26	GND	S9074 gnd		B26	RET3P	Imon		C26	IMONPS
SFET2d	A32	A27	MONP4	SFET2c	A32	B27	MONP3	Imon		C27	IMONPE
SFET2a	A32	A28	MONP1	SFET2b	A32	B28	MONP2			C28	GND
S9074		A29	+3V3P	chassis		B29	CHASGND	LeCroy		C29	NLBDP
		A30	GND	chassis		B30	CHASGND	LeCroy		C30	PLBDP
SPT2	A27	A31	FTPCK	S9074		B31	+3V3P	LeCroy		C31	PLBCLKP
SPT2	A28	A32	FTPJ	S9074		B32	+3V3P	LeCroy		C32	NLBCLKP

Table 13. SDR2 primary VME connector. Several SPT2 pins refer to the SFEC boards (see tables 11 and 12). Pins connected to the secondary VME connector of SDR2 are related to the non-redundant SFEC boards (via SPT2 VME connectors).

Other board pin		SDR2 pin/signal		Other board pin		SDR2 pin/signal		Other board pin		SDR2 pin/signal	
SFEA2	A5	A1	TWS5DO	SFEA2	A4	B1	TWS5SI	SFEA2	A3	C1	TWS5DI
SFEA2	A6	A2	TWS5SO	SFET2d	A4	B2	TWS4SI	SFET2d	A3	C2	TWS4DI
SFET2d	A5	A3	TWS4DO	SFET2c	A4	B3	TWS3SI	SFET2c	A3	C3	TWS3DI
SFET2d	A6	A4	TWS4SO	SFET2a	A4	B4	TWS1SI	SFET2a	A3	C4	TWS1DI
SFET2c	A5	A5	TWS3DO	SFET2b	A4	B5	TWS2SI	SFET2b	A3	C5	TWS2DI
SFET2c	A6	A6	TWS3SO	SPT2	A30	B6	TWS6SI	SPT2	A29	C6	TWS6DI
SFET2a	A5	A7	TWS1DO			B7	GND			C7	GND
SFET2a	A6	A8	TWS1SO			B8	GND			C8	GND
		A9	GND	SFET2b	A6	B9	TWS2SO	SFET2b	A5	C9	TWS2DO
SFEA2	A29	A10	CSS5	SPT2	A32	B10	TWS6SO	SPT2	A31	C10	TWS6DO
		A11	spare	SFET2d	A29	B11	CSS4	SFET2c	A29	C11	CSS3
SPT2	B23	A12	CSS6	SFET2a	A29	B12	CSS1	SFET2b	A29	C12	CSS2
		A13	GND	SPT2	B18	B13	CWS7S	SPT2	B16	C13	CWS7D
SFET2a	A2	A14	CTRLS1	SPT2	B21	B14	CWS7S	SPT2	B20	C14	CWS7D
		A15	spare	VME prim.	B15	B15	CWS6S	VME prim.	C15	C15	CWS6D
SFET2b	A2	A16	CTRLS2	VME prim.	B16	B16	CWS6S	VME prim.	C16	C16	CWS6D
		A17	spare	SFEA2	A31	B17	CWS5S	SFEA2	A30	C17	CWS5D
		A18	spare	SFET2d	A31	B18	CWS4S	SFET2d	A30	C18	CWS4D
SPT2	A25	A19	CTRLS6	SFET2c	A31	B19	CWS3S	SFET2c	A30	C19	CWS3D
		A20	spare	SFET2b	A31	B20	CWS2S	SFET2b	A30	C20	CWS2D
SPT2	C25	A21	CTRLS7	SFET2a	A31	B21	CWS1S	SFET2a	A30	C21	CWS1D
		A22	spare	SFET2c	A2	B22	CTRLS3	SPT2	C27	C22	MONS7
SFEA2	A2	A23	CTRLS5	SFET2d	A2	B23	CTRLS4	SPT2	A27	C23	MONS6
SFE*	A10	A24	LV1SA	SFE*	A9	B24	LV1SB	SFEA2	A32	C24	MONS5
S9074 gnd		A25	RET3S	S9074 gnd		B25	RET3S	Imon		C25	IMONSD
		A26	GND	S9074 gnd		B26	RET3S	Imon		C26	IMONSS
SFET2d	A32	A27	MONS4	SFET2c	A32	B27	MONS3	Imon		C27	IMONSE
SFET2a	A32	A28	MONS1	SFET2b	A32	B28	MONS2			C28	GND
S9074		A29	+3V3S	chassis		B29	CHASGND	LeCroy		C29	NLBDS
		A30	GND	chassis		B30	CHASGND	LeCroy		C30	PLBDS
SPT2	A5	A31	FTSL	S9074		B31	+3V3S	LeCroy		C31	PLBCLKS
SPT2	A6	A32	FTSM	S9074		B32	+3V3S	LeCroy		C32	NLBCLKS

Table 14. SDR2 secondary VME connector. Several SPT2 pins refer to the SFEC boards (see tables 11 and 12). Pins connected to the primary VME connector of SDR2 are related to the non-redundant SFEC boards (via SPT2 VME connectors).

Other board pin	SPT2 pin/signal	Other board pin	SPT2 pin/signal	Other board pin	SPT2 pin/signal
SDR2	A18	A1	CTRL1PT	S9074	B1 +3V3P
SDR2	A19	A2	CTRL2PT	S9074	B2 +3V3P
SDR2	C23	A3	MONPT	S9074	B3 +3V3P
		A4	GND	S9074 gnd	B4 RET3P
SDR2	C6	A5	TWPDO	S9074 gnd	B5 RET3P
SDR2	B6	A6	TWPSO	S9074 gnd	B6 RET3P
SDR2	C10	A7	TWPDI		B7 GND
SDR2	B10	A8	TWPSI	chassis	B8 CHASGND
SFET2a	A17	A9	HTP1		B9 CS7P
SFET2a	A18	A10	SHTP1	SDR2	A12 B10 CS7S
SFET2a	A19	A11	HTP2		B11 CW8DP
SFET2a	A20	A12	SHTP2	SDR2	C15 B12 CW8DS
SFET2a	A21	A13	HTP3		B13 CW8SP
SFET2a	A22	A14	SHTP3	SDR2	B15 B14 CW8SS
SFET2a	A23	A15	HTP4		B15 CW9DP
SFET2a	A24	A16	SHTP4	SDR2	C16 B16 CW9DS
SFET2b	A17	A17	HTP5		B17 CW9SP
SFET2b	A18	A18	SHTP5	SDR2	B16 B18 CW9SS
SFET2b	A19	A19	HTP6		B19 GND
SFET2b	A20	A20	SHTP6		B20 GND
SFET2b	A21	A21	HTP7		B21 GND
SFET2b	A22	A22	SHTP7		B22 GND
SFET2b	A23	A23	HTP8		B23 GND
SFET2b	A24	A24	SHTP8		B24 GND
		A25	GND	chassis	B25 CHASGND
		A26	GND		B26 GND
SDR2	A31	A27	FTPJ2	S9052	B27 -5V6P
SDR2	A32	A28	FTPJ2	S9052	B28 -5V6P
SFET2a	C31	A29	FTPJ5	S9052 gnd	B29 RET5P
SFET2a	C32	A30	FTPJ5	S9052 gnd	B30 RET5P
SFET2b	C31	A31	FTPJ1	S9052	B31 +5V6P
SFET2b	C32	A32	FTPJ1	S9052	B32 +5V6P
SDR2	A20	C1	CTRL1PC	SDR2	A20 C1 CTRL1PC
SDR2	A21	C2	CTRL2PC	SDR2	A21 C2 CTRL2PC
SDR2	C22	C3	MONPC	SDR2	C22 C3 MONPC
		C4	GND		C4 GND
SFET2d	C8	C5	HTP17	SFET2d	C8 C5 HTP17
SFET2d	C9	C6	SHTP17	SFET2d	C9 C6 SHTP17
SFET2c	C8	C7	HT18P	SFET2c	C8 C7 HT18P
SFET2c	C9	C8	SHTP18	SFET2c	C9 C8 SHTP18
SFET2d	A17	C9	HTP9	SFET2d	A17 C9 HTP9
SFET2d	A18	C10	SHTP9	SFET2d	A18 C10 SHTP9
SFET2d	A19	C11	HTP10	SFET2d	A19 C11 HTP10
SFET2d	A20	C12	SHTP10	SFET2d	A20 C12 SHTP10
SFET2d	A21	C13	HTP11	SFET2d	A21 C13 HTP11
SFET2d	A22	C14	SHTP11	SFET2d	A22 C14 SHTP11
SFET2d	A23	C15	HTP12	SFET2d	A23 C15 HTP12
SFET2d	A24	C16	SHTP12	SFET2d	A24 C16 SHTP12
SFET2c	A17	C17	HTP13	SFET2c	A17 C17 HTP13
SFET2c	A18	C18	SHTP13	SFET2c	A18 C18 SHTP13
SFET2c	A19	C19	HTP14	SFET2c	A19 C19 HTP14
SFET2c	A20	C20	SHTP14	SFET2c	A20 C20 SHTP14
SFET2c	A21	C21	HTP15	SFET2c	A21 C21 HTP15
SFET2c	A22	C22	SHTP15	SFET2c	A22 C22 SHTP15
SFET2c	A23	C23	HTP16	SFET2c	A23 C23 HTP16
SFET2c	A24	C24	SHTP16	SFET2c	A24 C24 SHTP16
		C25	GND		C25 GND
		C26	GND		C26 GND
SFEA2	C31	C27	FTPJ4	SFEA2	C31 C27 FTPJ4
SFEA2	C32	C28	FTPJ4	SFEA2	C32 C28 FTPJ4
SFET2d	C31	C29	FTPJ6	SFET2d	C31 C29 FTPJ6
SFET2d	C32	C30	FTPJ6	SFET2d	C32 C30 FTPJ6
SFET2c	C31	C31	FTPJ3	SFET2c	C31 C31 FTPJ3
SFET2c	C32	C32	FTPJ3	SFET2c	C32 C32 FTPJ3

Table 15. SPT2 primary VME connector.

Other board pin	SPT2 pin/signal	Other board pin	SPT2 pin/signal	Other board pin	SPT2 pin/signal
SFET2b	C1	A1	FTSL5	S9074	B1 +3V3S
SFET2b	C2	A2	FTSM5	S9074	B2 +3V3S
SFET2a	C1	A3	FTSL1	S9074	B3 +3V3S
SFET2a	C2	A4	FTSM1	S9074 gnd	B4 RET3S
SDR2	A31	A5	FTSL2	S9074 gnd	B5 RET3S
SDR2	A32	A6	FTSM2	S9074 gnd	B6 RET3S
		A7	GND		B7 GND
		A8	GND	chassis	B8 CHASGND
SFET2a	A17	A9	HTS1		B9 +5VHOT
SFET2a	A18	A10	SHTS1		B10 +5VHOT
SFET2a	A19	A11	HTS2		B11 +5VHOT
SFET2a	A20	A12	SHTS2		B12 RET5HOT
SFET2a	A21	A13	HTS3		B13 RET5HOT
SFET2a	A22	A14	SHTS3		B14 GND
SFET2a	A23	A15	HTS4		B15 CW6DP
SFET2a	A24	A16	SHTS4	SDR2 C13	B16 CW6DS
SFET2b	A17	A17	HTS5		B17 CW6SP
SFET2b	A18	A18	SHTS5	SDR2 B13	B18 CW6SS
SFET2b	A19	A19	HTS6		B19 CW7DP
SFET2b	A20	A20	SHTS6	SDR2 C14	B20 CW7DS
SFET2b	A21	A21	HTS7	SDR2 B14	B21 CW7SP
SFET2b	A22	A22	SHTS7		B22 CW7SS
SFET2b	A23	A23	HTS8	SDR2 A12	B23 CS6P
SFET2b	A24	A24	SHTS8		B24 CS6S
SDR2	A18	A25	CTRL1ST	chassis	B25 CHASGND
SDR2	A19	A26	CTRL2ST		B26 GND
SDR2	C23	A27	MONST	S9052	B27 -5V6S
		A28	GND	S9052	B28 -5V6S
SDR2	C6	A29	TWSDO	S9052 gnd	B29 RET5S
SDR2	B6	A30	TWSSO	S9052 gnd	B30 RET5S
SDR2	C10	A31	TWSDI	S9052	B31 +5V6S
SDR2	B10	A32	TWSSI	S9052	B32 +5V6S
SFET2c	C1	C1	FTSL6		
SFET2c	C2	C2	FTSM6		
SFET2d	C1	C3	FTSL3		
SFET2d	C2	C4	FTSM3		
SFEA2	C1	C5	FTSL4		
SFEA2	C2	C6	FTSM4		
		C7	GND		
		C8	GND		
SFET2d	A17	C9	HTS9		
SFET2d	A18	C10	SHTS9		
SFET2d	A19	C11	HTS10		
SFET2d	A20	C12	SHTS10		
SFET2d	A21	C13	HTS11		
SFET2d	A22	C14	SHTS11		
SFET2d	A23	C15	HTS12		
SFET2d	A24	C16	SHTS12		
SFET2c	A17	C17	HTS13		
SFET2c	A18	C18	SHTS13		
SFET2c	A19	C19	HTS14		
SFET2c	A20	C20	SHTS14		
SFET2c	A21	C21	HTS15		
SFET2c	A22	C22	SHTS15		
SFET2c	A23	C23	HTS16		
SFET2c	A24	C24	SHTS16		
SDR2	A20	C25	CTRL1SC		
SDR2	A21	C26	CTRL2SC		
SDR2	C22	C27	MONSC		
		C28	GND		
SFET2c	A25	C29	HTS17		
SFET2c	A26	C30	SHTS17		
SFET2d	A25	C31	HTS18		
SFET2d	A26	C32	SHTS18		

Table 16. SPT2 secondary VME connector. The 3.3 V line feeding the SFEC boards is obtained from the 5.1 V (always hot) line.

B.4. SFET2

Use	Pin	Signal	Use	Pin	Signal	Use	Pin	Signal
on/off	A1	CTRL1P		B1	GND		C1	GND
on/off	A2	CTRL2P		B2	GND		C2	GND
TOFwire	A3	TWPDO		B3	GND		C3	GND
TOFwire	A4	TWPSO	S9074	B4	+3V3P	S9074	C4	+3V3P
TOFwire	A5	TWPDI	S9074	B5	+3V3P	S9074	C5	+3V3P
TOFwire	A6	TWPSI		B6	GND	HT 5	C6	HTP5
	A7	GND		B7	GND	SHT 5	C7	SHTP5
	A8	GND		B8	GND		C8	GND
LVL1	A9	LV1PB		B9	GND		C9	GND
LVL1	A10	LV1PA		B10	GND		C10	GND
	A11	GND		B11	GND		C11	GND
	A12	GND		B12	GND		C12	GND
	A13	GND		B13	GND		C13	GND
	A14	GND		B14	GND		C14	GND
	A15	GND		B15	GND		C15	GND
	A16	GND		B16	GND		C16	GND
HT 1	A17	HTP1		B17	GND		C17	GND
SHT 1	A18	SHTP1		B18	GND		C18	GND
HT 2	A19	HTP2		B19	GND		C19	GND
SHT 2	A20	SHTP2		B20	GND		C20	GND
HT 3	A21	HTP3		B21	GND		C21	GND
SHT 3	A22	SHTP3		B22	GND		C22	GND
HT 4	A23	HTP4		B23	GND		C23	GND
SHT 4	A24	SHTP4		B24	GND		C24	GND
	A25	GND	S9052	B25	-5V6P	S9052	C25	-5V6P
	A26	GND	S9052	B26	-5V6P	S9052	C26	-5V6P
	A27	GND		B27	GND		C27	GND
	A28	GND	S9052	B28	+5V6P	S9052	C28	+5V6P
strobe	A29	CSP	S9052	B29	+5V6P	S9052	C29	+5V6P
charge	A30	CWPD		B30	GND		C30	GND
charge	A31	CWPS		B31	GND	FT	C31	FTPJ
status	A32	MONP		B32	GND	FT	C32	FTPJ

Table 17. SFET2 primary VME connector pin-out.

Use	Pin	Signal	Use	Pin	Signal	Use	Pin	Signal
on/off	A1	CTRL1S		B1	GND	FT	C1	FTSL
on/off	A2	CTRL2S		B2	GND	FT	C2	FTSM
TOFwire	A3	TWSDO		B3	GND		C3	GND
TOFwire	A4	TWSSO	S9074	B4	+3V3S	S9074	C4	+3V3S
TOFwire	A5	TWSDI	S9074	B5	+3V3S	S9074	C5	+3V3S
TOFwire	A6	TWSSI		B6	GND		C6	GND
	A7	GND		B7	GND		C7	GND
	A8	GND		B8	GND		C8	GND
LVL1	A9	LV1SB		B9	GND		C9	GND
LVL1	A10	LV1SA		B10	GND		C10	GND
	A11	GND		B11	GND		C11	GND
	A12	GND		B12	GND		C12	GND
	A13	GND		B13	GND		C13	GND
	A14	GND		B14	GND		C14	GND
	A15	GND		B15	GND		C15	GND
	A16	GND		B16	GND		C16	GND
HT 1	A17	HTS1		B17	GND		C17	GND
SHT 1	A18	SHTS1		B18	GND		C18	GND
HT 2	A19	HTS2		B19	GND		C19	GND
SHT 2	A20	SHTS2		B20	GND		C20	GND
HT 3	A21	HTS3		B21	GND		C21	GND
SHT 3	A22	SHTS3		B22	GND		C22	GND
HT 4	A23	HTS4		B23	GND		C23	GND
SHT 4	A24	SHTS4		B24	GND		C24	GND
HT 5	A25	HTS5	S9052	B25	-5V6S	S9052	C25	-5V6S
SHT 5	A26	SHTS5	S9052	B26	-5V6S	S9052	C26	-5V6S
	A27	GND		B27	GND		C27	GND
	A28	GND	S9052	B28	+5V6S	S9052	C28	+5V6S
strobe	A29	CSS	S9052	B29	+5V6S	S9052	C29	+5V6S
charge	A30	CWSD		B30	GND		C30	GND
charge	A31	CWSS		B31	GND		C31	GND
status	A32	MONS		B32	GND		C32	GND

Table 18. SFET2 secondary VME connector pin-out.

B.5. SFEA2

Use	Pin	Signal	Use	Pin	Signal	Use	Pin	Signal
on/off	A1	CTRL1P	S9052	B1	-5V6P		C1	GND
on/off	A2	CTRL2P	S9052	B2	-5V6P		C2	GND
TOFwire	A3	TWPDO	S9052	B3	-5V6P		C3	GND
TOFwire	A4	TWPSO	S9074	B4	GND		C4	GND
TOFwire	A5	TWPDI	S9074	B5	GND		C5	GND
TOFwire	A6	TWPSI	S9074	B6	GND		C6	GND
	A7	GND	S9074	B7	+3V3P		C7	GND
	A8	GND	S9074	B8	+3V3P		C8	Floating
	A9	LV1PB	S9074	B9	+3V3P		C9	Floating
	A10	LV1PA	S9074gnd	B10	RET3P		C10	GND
	A11	GND	S9074gnd	B11	RET3P		C11	GND
	A12	GND	S9074gnd	B12	RET3P		C12	GND
	A13	GND	S9052	B13	+5V6P		C13	GND
	A14	GND	S9052	B14	+5V6P		C14	GND
	A15	GND	S9052	B15	+5V6P		C15	GND
	A16	GND	chassis	B16	CHASGND		C16	GND
	A17	Floating	S9052gnd	B17	RET5P		C17	GND
	A18	Floating	S9052gnd	B18	RET5P		C18	GND
	A19	Floating	S9052gnd	B19	RET5P		C19	GND
	A20	Floating		B20	GND		C20	GND
	A21	Floating		B21	GND		C21	GND
	A22	Floating		B22	GND		C22	GND
	A23	Floating		B23	GND		C23	GND
	A24	Floating		B24	GND		C24	GND
	A25	GND		B25	GND		C25	GND
	A26	GND		B26	GND		C26	GND
	A27	GND		B27	GND		C27	GND
	A28	GND		B28	GND		C28	GND
strobe	A29	CSP		B29	GND		C29	GND
charge	A30	CWPD		B30	GND		C30	GND
charge	A31	CWPS		B31	GND	FT	C31	FTPJ
status	A32	MONP		B32	GND	FT	C32	FTPJ

Table 19. SFEA2 primary VME connector pin-out.

Use	Pin	Signal	Use	Pin	Signal	Use	Pin	Signal
on/off	A1	CTRL1S	S9052	B1	+5V6S		C1	GND
on/off	A2	CTRL2S	S9052	B2	+5V6S		C2	GND
TOFwire	A3	TWSDO	S9052	B3	+5V6S		C3	GND
TOFwire	A4	TWSSO	S9074	B4	+5V1S		C4	GND
TOFwire	A5	TWSDI	S9074	B5	+5V1S		C5	GND
TOFwire	A6	TWSSI	S9074	B6	+5V1S		C6	GND
	A7	GND	S9074	B7	+3V3S		C7	GND
	A8	GND	S9074	B8	+3V3S		C8	Floating
	A9	LV1SB	S9074	B9	+3V3S		C9	Floating
	A10	LV1SA	S9074gnd	B10	RET3S		C10	GND
	A11	GND	S9074gnd	B11	RET3S		C11	GND
	A12	GND	S9074gnd	B12	RET3S		C12	GND
	A13	GND	S9052	B13	-5V6S		C13	GND
	A14	GND	S9052	B14	-5V6S		C14	GND
	A15	GND	S9052	B15	-5V6S		C15	GND
	A16	GND	chassis	B16	CHASGND		C16	GND
	A17	Floating	S9052gnd	B17	RET5S		C17	GND
	A18	Floating	S9052gnd	B18	RET5S		C18	GND
	A19	Floating	S9052gnd	B19	RET5S		C19	GND
	A20	Floating		B20	GND		C20	GND
	A21	Floating		B21	GND		C21	GND
	A22	Floating		B22	GND		C22	GND
	A23	Floating		B23	GND		C23	GND
	A24	Floating		B24	GND		C24	GND
	A25	GND		B25	GND		C25	GND
	A26	GND		B26	GND		C26	GND
	A27	GND		B27	GND		C27	GND
	A28	GND		B28	GND		C28	GND
strobe	A29	CSS		B29	GND		C29	GND
charge	A30	CWSD		B30	GND		C30	GND
charge	A31	CWSS		B31	GND	FT	C31	FTSL
status	A32	MONS		B32	GND	FT	C32	FTSM

Table 20. SFEA2 secondary VME connector pin-out.

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