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ScintEle–02 v0.9

The AMS-02 scintillator front-end electronics

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ABSTRACT

The AMS-02 scintillator front-end electronics (the SFET2, SFEA2 and SFEC boards) principles are described in this document. In addition, the pre-trigger boards SPT2 is also considered.

TO DO:

- Fix input divider on SFET (SFEA).
- Check SFEC FM parameters.
- Fix temperature format.
- Check SPT2 protocol.

Contents

1. Document history

Changes since version 0.26 (Nov. 8, 2005)

- FT active high on backplane.
- Changed temperature word format.

Changes since version 0.25 (Oct. 21, 2005)

- Changed SFET/SFEA data formats.
- Completed SPT2 description.

Changes since version 0.18 (8 Apr 2005)

- Fixed ACC inputs to 50 Ohm coax.
- Changed standard for SPT2 (S)HT inputs.
- Changed data formats.
- Fixed SPT2 output signal widths.

Changes since version 0.15 (3 Sep 2004)

- Changed time and charge data format.

Changes since version 0.13 (1 Aug 2004)

- Changed SFET time data format.
- Fixed minima for thresholds.
- Added charge data format.

Changes since version 0.11 (27 Jul 2004)

- Changed SFET time data format.

2. The AMS-02 S-crate

The AMS-02 detector eletronics boards are distributed among different crates. The four "scintillators crates" or S-crates host the front-end and slow control boards of the time of flight (TOF) and anticoincidence (ACC) systems. In addition, each crate provides the high voltage lines that feed the TOF and ACC phototubes, and hosts the "pre-trigger" logics preceding the trigger boxes JLVL1A and JLVL1B.

Each S-crate contains the same number and type of boards: one scintillator data reduction redundant unit called SDR2, four scintillator front-end TOF redundant boards called SFET2, one scintillator front-end ACC redundant board called SFEA2, one redundant scintillator pre-trigger board (SPT2). The scintillator front-end charge (SFEC) boards are not redundant and are placed in the TOF enclosing box. They are connected to the S-crate with twisted-pairs cables. More details are given in [1].

The SFET2 and SFEA2 front-end boards and the SPT2 board are connected to the SDR2 through dedicated serial lines using the TOFwire protocol [2], whereas digitized charge data follow separate links [1].

There is no connection between the two halves of the same board, to ensure the complete double redundancy of the S-crate: during normal conditions, at any given time only half of the crate is powered. The only exception is that both primary and secondary SDR2 halves must be connected to the same SFEC boards, that must also be powered by both halves of the DC/DC converters [1]. The primary and secondary low-voltage (LV) lines are summed together inside SPT2, before reaching the SFECs.

In the following we will speak only about the "hot" modules, i.e. those modules that are actually powered.

3. The time measurement

The analog signals going to the time measurement units are compared to three fixed thresholds, called "low threshold" (LT, roughly −20 mV), "high threshold" (HT, −60 mV), and "super-high threshold" (SHT, −350 mV) (figure 1).

The digital signals produced by the comparators will be used to start the time measurement (LT), to send a "charged particle" signal to the trigger logics (HT), and to send a "big charge" signal to the trigger logics (SHT). In addition, LT and HT are used by the LeCroy MTD 135 TDC, that has two buffers per channel: the "time" and "history" buffers.

In order to improve the time resolution, the time elapsed between the passing of the LT and the arrival of the fast trigger (FT) (using the front numbering of figure 1, this time is "4–3") is multiplied by a factor $M = 25$–30 ("time expansion") and is measured again (time "3–1" in figure 1). If the intrinsic TDC resolution is σ_{TDC} and the fluctuations on M are negligible, the final time resolution after the time expansion is $\sigma \approx \sigma_{\mathrm{TDC}}/M$. Any instability of the time expansion factor M will result in a higher σ.

The time expansion technique is the following: in order to measure the time Δt elapsed

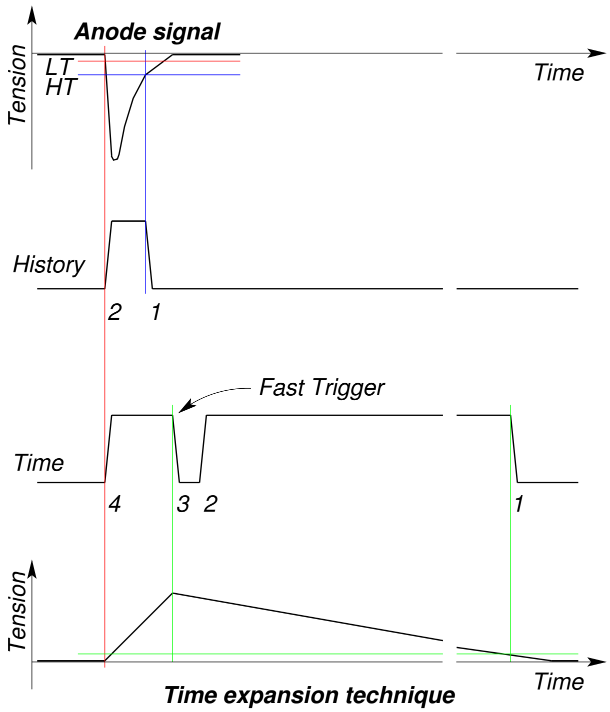

Figure 1. Schema of the time measurement. The analog signal is compared to fixed thresholds, and the precision of the time measurement is enhanced by the time expansion technique.

between the LT and the FT ("4–3" in figure 1), a capacitor is charged linearly during this time. Upon the FT arrival, it starts discharging linearly[1] on a circuit with a longer characteristic time. The triangular-shaped voltage law of the capacitor is compared with a fixed threshold, and the "expanded time" is given by the delay between the last crossing point and the LT ("4–1" in figure 1). If M is the ratio between "3–1" and "4–3", the total time "4–1" is equal to $(M+1)\Delta t$.

4. The fast trigger generation

The fast trigger is the reference time of the event recorded by the data acquisition (DAQ) AMS-02 electronics. It will be generated when at least one counter side produces a pulse passing the HT in 3 planes of the TOF system. Higher thresholds (super-high threshold, SHT) are used to flag events with large energy losses in the TOF scintillators, presumably produced by particles with charge $Z \geq 2$.

There are two identical trigger boards, JLV1A and JLV1B, for redundancy [3]. They do not operate directly upon the logical signals produced when the HTs are passed. Instead, these signals are first combined together inside each S-crate by the SPT2 board [4], and the results are sent to the JLV1x.

[1] Current limiters are used to produce a linear charge/discharge.

Basically, the SPT2 receives the logical signals corresponding to HT and SHT of each TOF channel read by its S-crate and makes few logical sums:

1. the OR of the HT of all counter sides of the first TOF half plane;
2. the OR of the HT of all counter sides of the second TOF half plane;

(these combinations are called “charged particle”, or CP, signals [5])

3. the OR of the HT of the central counter sides of the first TOF half plane;
4. the OR of the HT of the central counter sides of the second TOF half plane;

(these combinations are called “central charged particle”, or CT, signals)

5. the OR of the SHT of all counter sides of the first TOF half plane;
6. the OR of the SHT of all counter sides of the second TOF half plane;

(these combinations are called “particle with big charge”, or BZ, signals). The CP, CT and BZ are sent as LVDS active-low signals (250 ns minimum length) to JLV1A and JLV1B by the SPT2 board. The CP and CT signals will be used by the JLV1x boards to start the fast trigger for charged particles, whereas the BZ signals will be used to make the fast trigger for big Z particles [3].

The JLV1x boards send the FT and the level 1 trigger (LV1) signals (both LVDS, active-low, 320 ns) to the S-crates and receive the BUSY signals from them [5]. Whereas LV1 and BUSY signals are sent-to/received-by the SDR2 board, the FT signals are sent to the SPT2: each JLV1x sends 4 LVDS active-low FT signals on a multi-wire twisted cable ending with a 9-pins μD connector.

Figure 2 explains how the 4 + 4 FTAn and FTBn (with $n = 1 \ldots 4$), that are the fast trigger LVDS signals received from JLV1A and JLV1B on the front panel, active low, are combined into 2 + 2 (primary + secondary[2]) TTL3.3V FThA and FThB signals (h = P, S for primary, secondary), active high, that are used by each half of the S-crate. The latter signals are split into several lines (FTPhn, FTShn, h = P, S, $n = 1 \ldots 6$), and sent in pairs **[to the same backplane lines]** (i.e. FTPA1 goes to the same line as FTPB1, FTSA1 goes to the same line as FTSB1, et cetera). **FIX ME!**

5. The charge measurement

The anode and dynode signals produced when a charged particle crosses a scintillation counter by the TOF PMTs (very similar to ideal current sources) are short current pulses that are read on a 50 Ω resistor. The ACC anodes are also read using 50 Ω coaxial cables.

[2]Primary and secondary electronics are defined by the powering lines, that are different for the JLV1x and the S-crates.

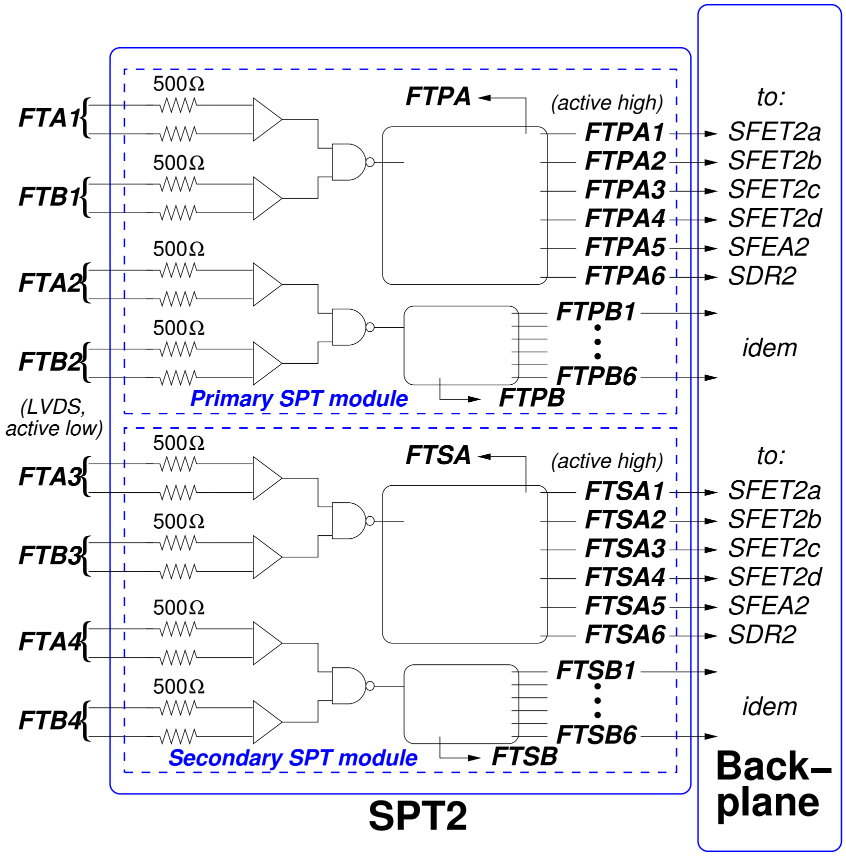

Figure 2. The FT signals (active low, LVDS) coming from both JLV1A and JLV1B are received by all S-crate boards (active high, TTL3.3V).

The time-integrated current pulse (i.e. the charge collected by the FE electronics) is proportional to the number of photons produced in the scintillator by the ionization losses of the charged particle, a function of the ion charge and velocity.

In order to measure the collected charge, the pulse is sent to a preamplifier and shaper analog integrated circuit [6] that transforms the few tens of ns long pulse into a much longer pulse ($\sim$ 1 µs long), whose maximum voltage is proportional to the integrated charge. A "sample-and-hold" technique is then used to keep memory of this maximum voltage (reached roughly 2 µs after the input pulse), which is sent to a linear ADC for the digitization.

The analog chip has two different scales (with gains "G1" and "G5" in the ratio 1:5) and is able to measure the charge of 16 independent input channels. After the sample-and-hold command is received, a multiplexer allows for the consecutive selection of the constant voltage of each channel. The first 16 levels correspond to input channels 1..16 in gain G1, then the 16 G5 levels are selected. Following each channel selection, the ADC takes about 1 µs to digitize its input. Two versions of the analog chip exist, with negative (for anodes) and positive (for dynodes) inputs.

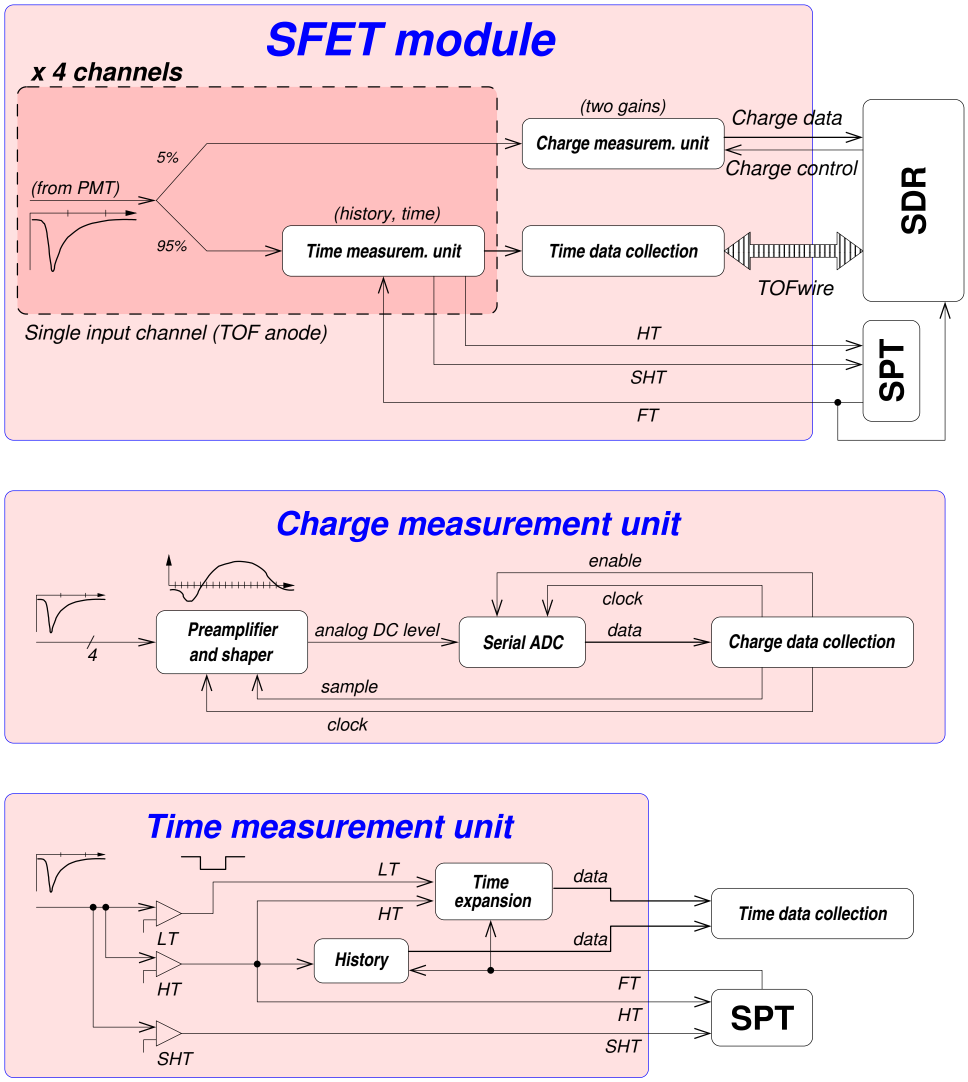

Figure 3. Block scheme of the SFET module.

6. The SFET module

The SFET2 board consists of two identical SFET modules, physically mounted on the same board. During normal operations, only one SFET module is powered. Each module is divided into two units: the time measurement unit and the charge measurement unit (figure 3).

The 4 analog input lines, carrying the TOF anode signals, are split with a passive divider into two paths: the bigger **[99.5%?]** fraction goes to the time measurement unit, whereas the smaller goes to the charge measurement unit. Figure 3 shows a scheme of the two measurement units. **FIX ME!**

The time measurement unit uses the time expansion technique explained in section 3. The

LeCroy MTD 135 TDC has two independent 16-fronts deep buffers for each input channel, called "history" and "time" buffer. The latter stores the four fronts of the time expansion and then freezes. However, it can contain additional pairs of elder fronts, produced by the crossing of the LT of pulses that are not followed by the FT within a maximum delay (FT must be received between 80 and 250 ns after the HT crossing). On the other hand, the history buffer is active even after the FT arrival, and keeps track of front pairs corresponding to the crossings of the HT.

The external clock frequency on the SFET2 is 100 MHz, but internally the TDC multiplies it by 8, obtaining 1.25 ns "ticks". Because the TDC has 14-bits words, the maximum depth of the buffers is about 20 μs. All TDC words express the number of 1.25 ns "ticks" elapsed between each front and the "common stop" (CS) signal, generated with a fixed delay after the FT arrival. The CS is produced using a linear capacitor discharge similar to that of the time expansion technique. The delay can be found by looking at the time corresponding to the FT (front 3 in figure 1), and is about 6.5 μs. Hence, the history buffer records all HT crossings since 13.5 μs before FT, until 6.5 μs after FT.

When a pulse passes the LT, the module waits at most $\Delta t_{\mathrm{max}} = 250$ ns for the FT arrival, then starts automatically the discharge of the time expansion capacitor. Hence, a pulse not followed by the FT within Δt_{max} makes the current channel busy for the time $\Delta t_{\mathrm{busy}} = (M + 1)\Delta t_{\mathrm{max}} =$ 6.2–7.5 μs (for $M = 25$–30) elapsed between the LT crossing and the complete discharge of the capacitor. However, no busy signal is sent out by the SFET2[3]. Rather, the time buffer must be scanned to check that any front elder than number 4, if present, is at least Δt_{busy} elder than FT. If a front is preceeding the LT by less than this time, the time expansion charging phase starts with an offset that will produce a longer delay with respect to the FT. Such events shall be rejected in the data analysis.

The history channel is useful to flag (eventually discard) offline events with other particles crossing the detector in the 6–7 μs following the FT: the charge integration process of the different AMS-02 subdetectors takes few microseconds, and additional particles could introduce systematic deviations in the charge measurements.

HT and SHT signals (active-low, 250 ns long) are sent to SPT2 via the backplane [1].

6.1. The time measurement

The TDC input lines are controlled by a programmable chip (Actel A54SX08A), whereas the data from all channels are collected by a bigger programmable chip (Actel A54SX32A), that is also in charge of communicating with the SDR module via a dedicated TOFwire connection [2].

SFET2/SFEA2 boards might have no TDC data for a given event. However, they have at least one TOFwire word to be transmitted to SDR2, encoding the temperature of the board itself. If TDC data are present, they are preceded by the temperature word [2].

[3] SDR2 also receives the FT (see figure 2), and shall use it to rise the busy signal [2].

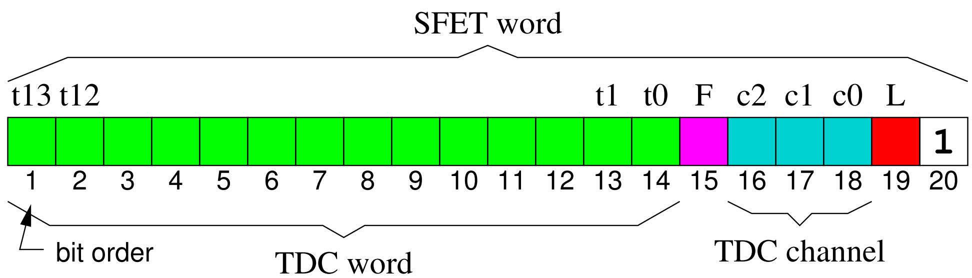

Figure 4. Output SFET time data format. The TDC word bits are "t13"…"t0" (most to least significant); F = 1 (0) means that the analog signal crossed downward (upward) the fixed threshold; the following three bits ("c2", "c1","c0") encode the channel number; L = 1 indicates that this is the last SFET word.

Data format. The SFET words are 20 bits long, always ending with one bit set to 1 (figure 4). The first 14 bits are the TDC word (most significant bit first). The TDC word is the integer number of clock ticks (1.25 ns period) elapsed between the considered front and the arrival of the common stop (CS). The next bit encodes the front type (F = 1 downward, or F = 0 upward)[4]. The next 3 bits contain the channel number, starting from the most significant bit, and are followed by a control bit that flags the last SFET word.

The output bits are 100 ns long, and there is a 100 ns delay between the end of a word and the following one. Hence, the SFET throughput is 1 word every 2.1 μs. The full communication protocol with SDR is explained in Ref. [2].

The number of TDC words is not known *a priori*: it can be anything from zero to the maximum = (no. of TDC channels) × (TDC buffer depth) = 8 × 16 = 128. However, normal events should have 6 TDC words (2 history and 4 time-expansion fronts) for every TOF channel recording a physical signal (produced by a charged particle crossing a scintillator), and 2 TDC words (history only) for ACC channels. In most events, a given SFET2/SFEA2 board will have data only for one input channel.

6.2. The charge measurement

Each SFET module has a FE chip for the anode charge measurement that reads the 4 input channels. The output of this chip is sent to the 12-bits AD7476 Analog Devices serial ADC, that is read by the control logics. Because all the SFE* modules have the same FE chip for the charge measurement, what follows is true for all SFE* modules.

The charge data read-out is carried on with the help of two functional units, called "charge control block" (CCB, on the SDR module) and "charge data collector" (CDC, on the SFE* modules) [7]. After receiving the FT signal, the CCB starts a sequence of digital strobes on several lines in parallel. Each line is read by a different CDC, a finite state machine that makes

[4]Offline one has to check that the words coming from a given channel have couples of fronts, and that the first one has F = 1 whereas the second has F = 0. Different successions can be produced by hardware problems.

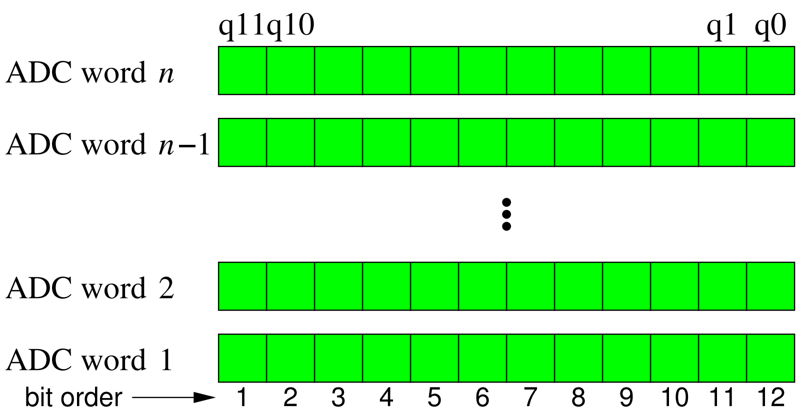

Figure 5. Output SFE* charge data format. The ADC 12-bits words are continuously transmitted following the reception of the charge strobes.

a step for each strobe it receives. Each CDC sends to the CCB the charge collected data as a bit stream, using as clock the charge strobes sent by CCB. The latter reads asynchronously all the charge links and writes the data in memory [2].

The physical lines going from the CCB to the CDCs are TTL3.3V lines on the S-crate backplane[5]. The charge data, reaching the CCB from the CDCs, are sent through a TTL3.3V data/strobe pair of backplane lines[6], whose XOR gives the asynchronous clock to the input routines of the CCB.

Data format. The charge words sent by SFEC, SFET and SFEA modules to the SDR module are 12 bits long, and are transmitted from the most to the least significant bit (figure 5). All charge words are sent as output one after the other, first to last channel, low gain (8.8×10^{-3} pC/ch) first, followed by high gain (G5 scale, with 0.176×10^{-3} pC/ch). **[MEASURE REAL pC/ch !!!]**

FIX ME!

If bit stream does not reach its end, a reset following a time-out of **[3 µs]** should be generated both on the SFE* module (i.e. by the CDC) **[and on the SDR module (i.e. by the CCB)]**.

FIX ME!
FIX ME!

6.3. Commands

Commands accepted by by SFET (and SFEA) modules are 6-bits long, the sixth bit always being equal to ‘1’. These commands are reported in table 1, where the possible answers (with 20-bits words) are also shown.

The answer to the “TestLink” command consists of the “echo” of the command itself, followed by its bit-wise negation, the error bit (e = ‘1’ means “error”), the most significant TDC

[5]Those reaching the SFECs are converted to LVDS inside the SPT2. See §8.

[6]Charge lines from SFECs are converted from LVDS to TTL3.3V on the SPT2 board. See §8.

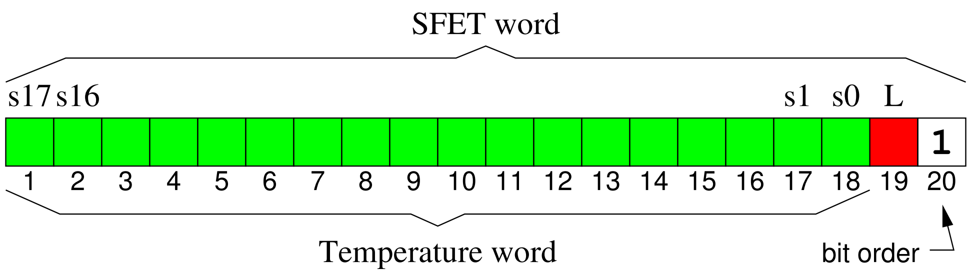

Figure 6. Output SFE* temperature data format. The temperature word is 18 bits long. If L = '1', this is also the last TOFwire word.

bits (bits 15 and 14, not used), and by the last DAC channel addressed by a "SetThreshold" command (not used).

The "Reset" command is not acknowledged. A "TestLink" command should be used to check the SFET/SFEA status. The normal DAQ command is "GetTDCdata", after which the board always transmit the temperature word (figure 6 **[format?]**), followed by all TDC words (if any). At the end of the output sequence, the TDC is reset and initialized again. To read only the board temperature, the "GetTemperature" command is used (the answer will have L = '1'). **FIX ME!**

Slow-control commands accepted by SFET (and SFEA) modules are about threshold settings. All such commands are followed by 16-bits words, ending with the bit "1", which encode the actual DAC settings for the selected channel.

The thresholds on SFET (and SFEA) modules are adjustable from a minimum value (set automatically at power-on) up to maximum values that are different between LT, HT and SHT. The tuning is done via 8-bits DACs: the four LT levels are controlled in couples, whereas HT and SHT values are individually tunable. The minimum values (step size) are: −10 mV (1 mV) for LT, −40 mV (2 mV) for HT, −120 mV (5 mV) for SHT.

Code	Command	Answer
`101011`	Test link	`101011010100ettccc11`
`000001`	Reset & initialize TDC	—
`010101`	Get TDC data & reset/init TDC	temperature + (opt.) TDC words
`011001`	Get temperature	temperature word
`110001`	Set low thresholds	—
`110011`	Set HT (& SHT) for channel 0	—
`110101`	Set HT (& SHT) for channel 1	—
`110111`	Set HT (& SHT) for channel 2	—
`111001`	Set HT (& SHT) for channel 3	—

Table 1. Accepted commands (6-bits words) by SFET/SFEA modules and answers (20-bit words). Threshold setting commands must be followed by one 16-bits word encoding the actual DAC settings.

7. The SFEA module

The SFEA2 board consist of two (primary/secondary) identical SFEA modules for redundancy. Each module reads four ACC anodes and two TOF anodes (not connected in the upper S-crates [1]).

The TOF channels are identical to the SFET module. The ACC analog signals are split in two parts: the lower fraction goes to the FE chip used to measure the charge of ACC and TOF channels, whereas the higher one is compared to one threshold only (instead of LT, HT and SHT). If the pulse passes the threshold, the TDC history buffer keeps track of the crossing time and a logical signal (LVDS, active-low, 120 ns long [5]) is sent to JLV1A and JLV1B from the front panel [1]. There is no time-expansion buffer for ACC channels.

The data format is the same as for the SFET module (see §6.1, §6.2 and §6.3).

8. The SFEC module

The SFEC board measures the charge collected by 10 TOF PMT dynodes. This board is not doubly redundant, however it contains two FE preamplifier and shaper analog chips (with positive inputs) and two linear ADCs, and each counter side will have a PMT connected to one FE chip and the other PMT connected to the other FE chip [1].

There is a single Actel A54SX08A programmed gate array for the two FE chips, that operates in the same way of SFET and SFEA modules [2]. The only difference is that there are two serial data lines carrying away the digital data independently for each FE chip, i.e. each strobe on the line coming from the CCB is used by the CDC routine, implemented in the SFEC control logics, to make two parallel steps. The control and data lines are LVDS lines. The strobe line from the CCB is converted from TTL3.3V to LVDS on the SPT2 board, before reaching the SFEC. Output data are sent to the SDR2 with the data/strobe technique via LVDS lines converted to TTL3.3V backplane lines on the SPT2 board.

The data format of each of the two output (data+strobe) lines is the same as for the SFET module (see §6.2).

9. The SPT module

The SPT module implements pre-trigger combinations of logical signals coming from SFET and SFEA modules, and sends the results to the trigger boards JLV1A and JLV1B [3], as stated in section 4. Each SPT module (primary, secondary) sends the output signals (CP, CT, BZ signals) to both trigger boards using LVDS connections.

Input signals are 8+10 HT and 8+10 SHT active-low, 250 ns long. For each input line, a 16-bits scaler counts the number of pulses received since the last scalers reset [8]. In addition, four registers are used to remember what input channel is active when the FT is generated ("trigger patterns"). Finally, four registers are used to mask out selectively each input line.

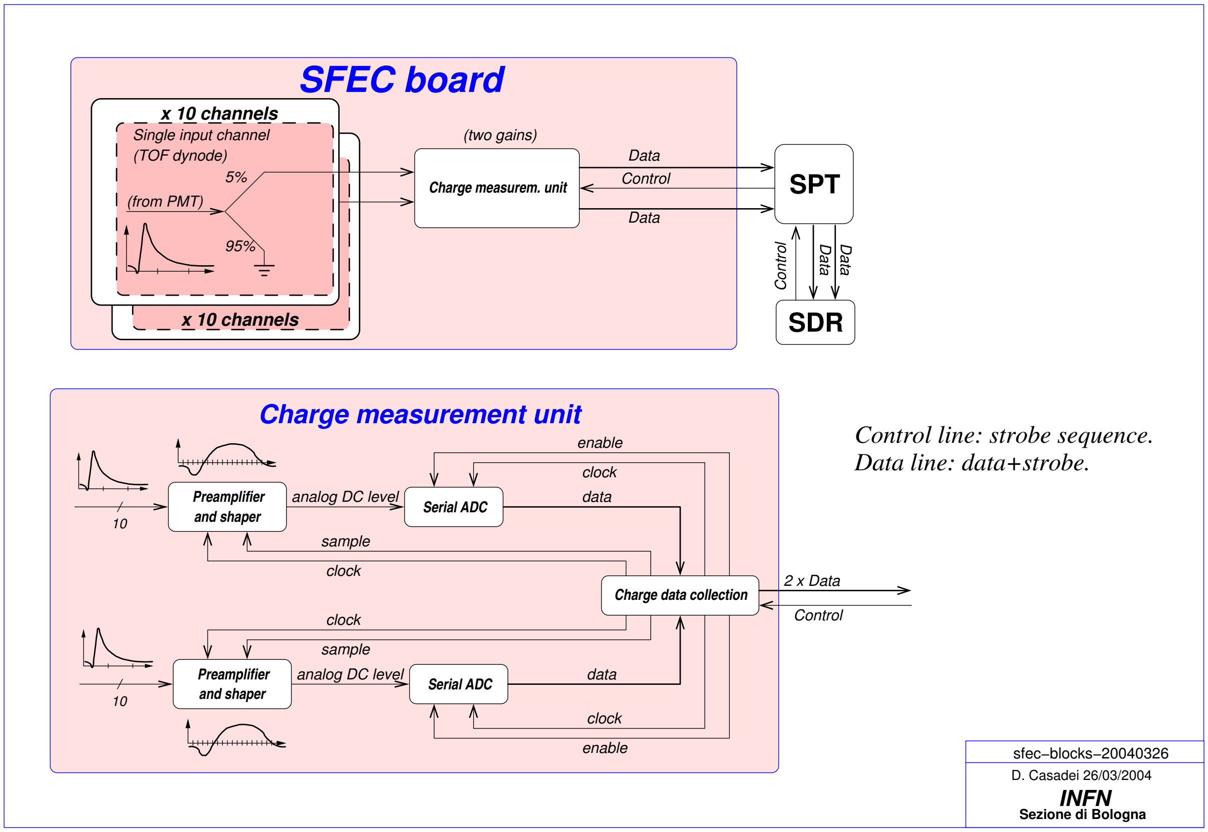

Figure 7. Block scheme of the SFEC module.

9.1. Trigger patterns

When the SPT module receives a FT, it writes the trigger patterns on the four registers [8] and it is ready to transmit their contents to SDR2. If a following FT comes before data have been transmitted, the newer patterns overwrite the old ones. **[CHECK!]** **FIX ME!**

Trigger patterns are written as output following the "GetData" command, but they can also be requested explicitly by issuing the "Read" command four times, one for each pattern [8]. **[CHECK!]** **FIX ME!**

[CHECK!!!!!] The data coming from SPT2 following the "GetData" SDR2 command are 4 16-bits words, encoding **FIX ME!**

1. HT trigger pattern (8 bits), first plane;
2. HT trigger pattern (10 bits), second plane;
3. SHT trigger pattern (8 bits), first plane;
4. SHT trigger pattern (10 bits), second plane.

The first counter is mapped to the least significant bit (bit 0) of the corresponding word, the second counter is mapped on bit 1, and so on. The last 8 (6) bits of each 16-bits word will be

FIX ME! zero ('1' meaning "signal received"). **[CHECK!]**

9.2. Trigger masks

Individual channels can be masked out of the trigger logics with the "SetMask" commands [8]. There are 6 trigger masks, for CP, CT and BZ logics acting on each half-plane set of inputs, which can also be read by issuing the "Read" command encoding the corresponding address [8]. The bit-channel mapping is the same as that of the trigger patterns reported in the previous section **[CHECK]**.

FIX ME!

9.3. Scalers

The "Read" command can also access to the scaler of each channel, when encoding the corresponding register address [8].

9.4. Other slow-control commands

The "Read" command can access few other registers, listed by Lin [8].

REFERENCES

[1]D. Casadei et al., "S-crate physical connections" v. 2.35, AMS Internal Note ScintEle–01, 2005, http://ams.cern.ch/AMS/Electronics/SubD/Scint/.

[2]D. Casadei et al., "AMS-02 scintillators data acquisition and slow control", AMS Internal Note ScintEle–03, 2005, in preparation.

[3]C.H. Lin, "Trigger Logics Design Specification", AMS Internal Note AMS-JT-JLV1-LOGIC-R01A, Jun 5, 2003, http://linch.home.cern.ch/linch/.

[4]A. Contin, "Local TOF trigger specifications", AMS-Bologna Internal Note Trigger-01, Dec 07, 2002.

[5]C.H. Lin, "Interface Control Document for Trigger System", AMS Internal Note AMS-JT-JLVL1-ICD-R04B, Jun 26, 2003, http://linch.home.cern.ch/linch/.

[6]L. Gallin-Martel, J. Pouxe, O. Rossetto, M. Yamouni, "A 16-channel analog integrated circuit for pulse processing", Nuclear Science, IEEE Transactions Vol. 49, Issue 4 (2002) 1798-1801.

[7]L. Villa, "L'elettronica di front-end del sistema TOF di AMS-02", Tesi di Laurea, Bologna, 2004.

[8]C.H. Lin, AMS Internal Note, Jul 12, 2005.