

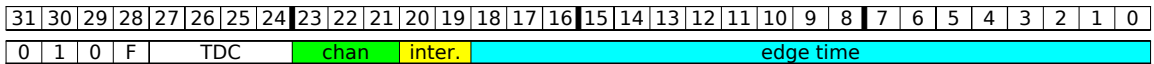
SFET2/SFEA2

Event data format – v. 3

D. Casadei 29-09-2006

SFET/A: HPTDC internal format

32-bits words (page 24 of hptdc_manual_ver2.2.pdf)

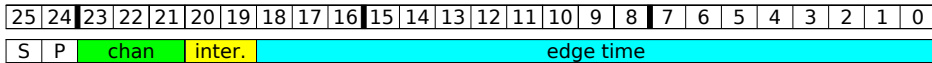


F = 0 (leading) or 1 (trailing edge)
inter. = least 2 significant bits of time measurements

Data serially transmitted to the FPGA

SFET/A: FPGA output time format

26-bits words



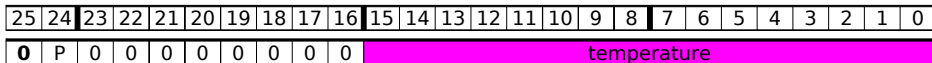
Edge time is left-shifted 2 positions, interpolated (hi-res) bits mapped into the lowest bits
S = 1 (last word for this link) or 0

P = parity bit. Parity must be even

Serial transmission: MSB (bit 25) first, LSB (bit 0) last; 80 ns/bit

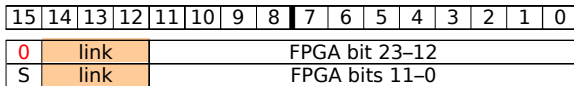
SFET/A: FPGA output temperature format

26-bits words



SDR2: Raw event buffer format

2 consecutive 16-bits words (most significant first)



S = 1 (last word for this link) or 0

board	link	hex
SFET2a	0 0 1	0x1
SFET2b	0 1 0	0x2
SFET2c	0 1 1	0x3
SFET2d	1 0 0	0x4
SFEA2	1 0 1	0x5

#	Example
1	0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 temp 15–12 temp0
2	0 0 0 1 temperature bits 11–0 temp1

9	0 1 0 1 0 0 0 0 0 0 0 0 0 0 0 temp 15–12 temp0
10	0 1 0 1 temperature bits 11–0 temp1
11	0 0 0 1 chan inter. edge time 18–12 time0
12	S 0 0 1 edge time 11–0 time1

19	0 1 0 1 chan inter. edge time 18–12 time0
20	S 1 0 1 edge time 11–0 time1