

SFET2_2006 SFEA2_2006 Specifications, Ver. 2



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SFET2 goals

- Provide logical signals to the trigger boxes JLV1x about:
 - Any charged particle (\rightarrow fast trigger, FT)
 - Particles with charge > 1 (\rightarrow special trigger, FTZ)
- Measure the time of counter hits related to the FT with the highest resolution as possible (\rightarrow TOF)
- Measure the integral of the analog pulses corresponding to such hits:
 - High resolution at low values (\rightarrow slewing corrections)
 - Highest dynamic range as possible (\rightarrow most abundant CR ions)
- Keep memory about hits produced by particles crossing the detector in a time window (at least) extending from $t_{FT} - 10 \mu s$ to $t_{FT} + 6 \mu s$ (\rightarrow effects on signal formation time of other detectors)

SFEA2 goals

- Provide logical signals to the trigger boxes JLV1x about hits produced by particles crossing ACC paddles in coincidence with TOF hits (→ avoid fake FT)
- Measure the integral of the pulses corresponding to such hits
- Measure the time (with respect to the FT) for these hits
- SFEA2 is functionally a subset of SFET2

The new TDC

- **HPTDC:** <http://micdigital.web.cern.ch/micdigital/hptdc.htm>
 - Radiation tolerant (developed for LHC) ball-grid array
 - 8 channels with 24.4 ps/count in very high resolution mode (25 ± 2 ps/count)
 - Differential non-linearity: +1.3, -0.7 bin (0.21 bin RMS)
 - Integral non-linearity: +3.5, -5.0 bin (2.1 bin RMS)
 - 21-bits time words (+ 3 bits for channel address)
 - 256-words L1 buffers
 - Maximum history $\approx 50 \mu\text{s}$
 - Adjustable dead time on each input (5, 10, 30, 100 ns)
- To be connected to a FPGA (Actel) for chip programming (JTAG) and data collection (serial link)

HPTDC architecture

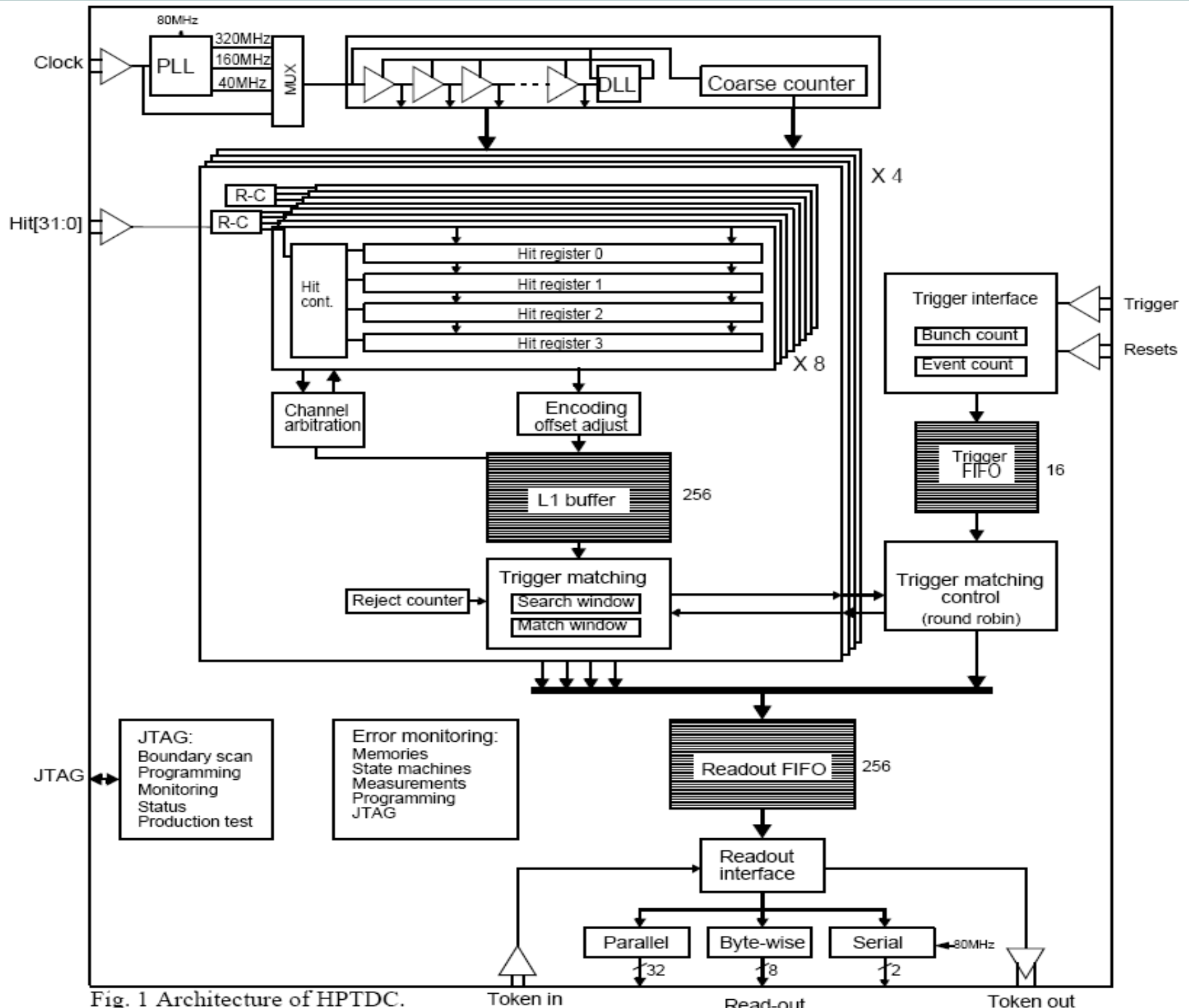


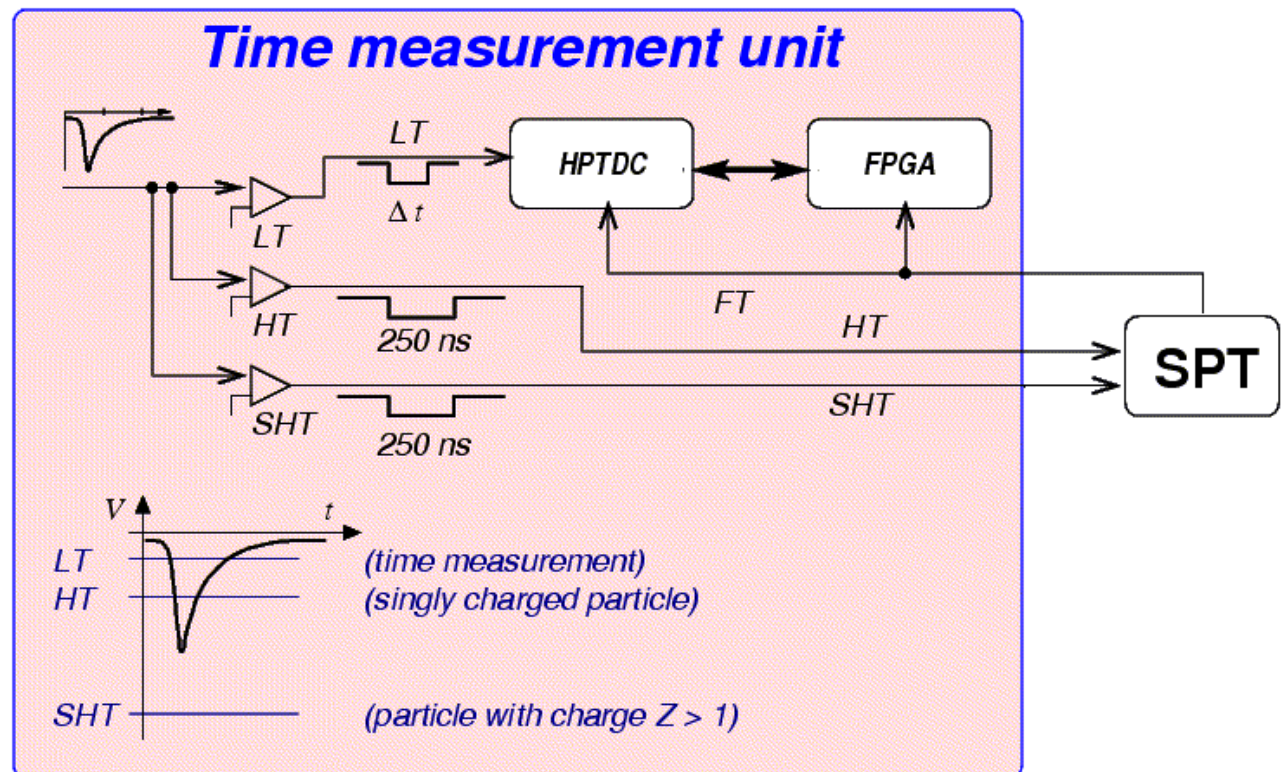
Fig. 1 Architecture of HPTDC.

Channels distribution (1)

- 4 ACC channels to SFEA2 (a board dedicated to ACC is needed for the trigger system cabling)
- 5 TOF channels to SFET2
- $4 \times \text{SFET2} + 1 \times \text{SFEA2} = 20 \text{ TOF} + 4 \text{ ACC}$ channels can be connected to each S-crate (we need 18 at most)

Thresholds (1)

- Low thresholds (LT) are the TDC inputs:
 - LT is at 10-20% V_{peak} to improve the time resolution
- High thresholds (HT) and super-high thresholds (SHT) are sent to the pre-trigger (SPT) module:
 - HT are used to produce the FT (aka FTC); SHT for FTZ
- Fast trigger (FT) goes to one TDC input too
- As in the old SFET2 design, LT could be produced by chance: we need to remember HT to keep track of real particles



Thresholds (2)

- FT and 5 TOF channels are sent to TDC \Rightarrow 2 inputs free
- To avoid discarding events with noisy hits inside the history window, **one should keep memory of HT** (in addition to LT):
 - Logical sum of the 5 HT to TDC (ch.6, **optional**)
 - Logical sum of the 5 SHT to TDC (ch. 7, **optional**)
- Examples:

TDC ch.	Name	SFET2_01	SFET2_32	TDC ch.	Name
0	202p			0	301n
1	204p			1	303n
2	206p			2	305n
3	208p			3	307n
4	---			4	309n
5	FT			5	FT
6	aux1			6	aux1
7	aux2			7	aux2

Thresholds (3)

- During offline analysis, if there are off-time (i.e. not correlated with the FT) hits in some LT channel, one has to search for corresponding hits in the sum(HT), in order to check that the hits correspond to a physical signal produced by a charged particle.
- The search has to be carried on in a narrow interval around the time of the LT hits (random correlations are statistically negligible provided that adjacent counters are not connected to the same board)

Channels distribution (2)

- The tables below report the channel assignment to the SFET2's placed into upper and lower S-crates.
- For each channel, the corresponding counter is reported (positive/negative side omitted) along with the corresponding output logical signals ordinal number n (SPT2 inputs are HT n and SHT n). <http://ams.cern.ch/AMS/Electronics/SubD/Scint/Docs/numbers-v5.2.pdf>

Upper	Ch. 1 (out thr.)		Ch. 2 (out thr.)		Ch. 3 (out thr.)		Ch. 4 (out thr.)		Ch. 5 (out thr.)	
SFET2a	201	T1	203	T2	205	T3	207	T4	---	---
SFET2b	202	T5	204	T6	206	T7	208	T8	---	---
SFET2c	101	T9	103	T10	105	T11	107	T12	---	T17
SFET2d	102	T13	104	T14	106	T15	108	T16	---	T18

Lower	Ch. 1 (out thr.)		Ch. 2 (out thr.)		Ch. 3 (out thr.)		Ch. 4 (out thr.)		Ch. 5 (out thr.)	
SFET2a	401	T1	403	T2	405	T3	407	T4	---	---
SFET2b	402	T5	404	T6	406	T7	408	T8	---	---
SFET2c	301	T9	303	T10	305	T11	307	T12	309	T17
SFET2d	302	T13	304	T14	306	T15	308	T16	310	T18

Thresholds (3)

- HT and SHT are formatted: logical signals 250 ns long
- HT & SHT are always active (no mask on SFET2)
- LT signals are not formed with a fixed width: the time-over-threshold (T_{ovT}) of the analog signal will determine the duration of the comparator output
- Normal events (1 MIP) have $T_{ovT} = 10-20$ ns (LT). High charges will have longer T_{ovT} ($T_{ovT} \sim \log Q$)
- Noise could induce very short glitches (few ns) in the LT comparators: they will be recorded by the TDC (as in AMS-01), in the corresponding LT channel. However, no related hit in $\text{sum}(\text{HT})$ will be found
- TDC inputs have adjustable dead time (default value will be 30 ns)

History and dead time

- **History:**

- All SFET2 LT and (**optional**) sum(HT), sum(SHT) hits inside the “history time window” are recorded.
- All SFEA2 hits above threshold and inside the “history time window” are recorded.

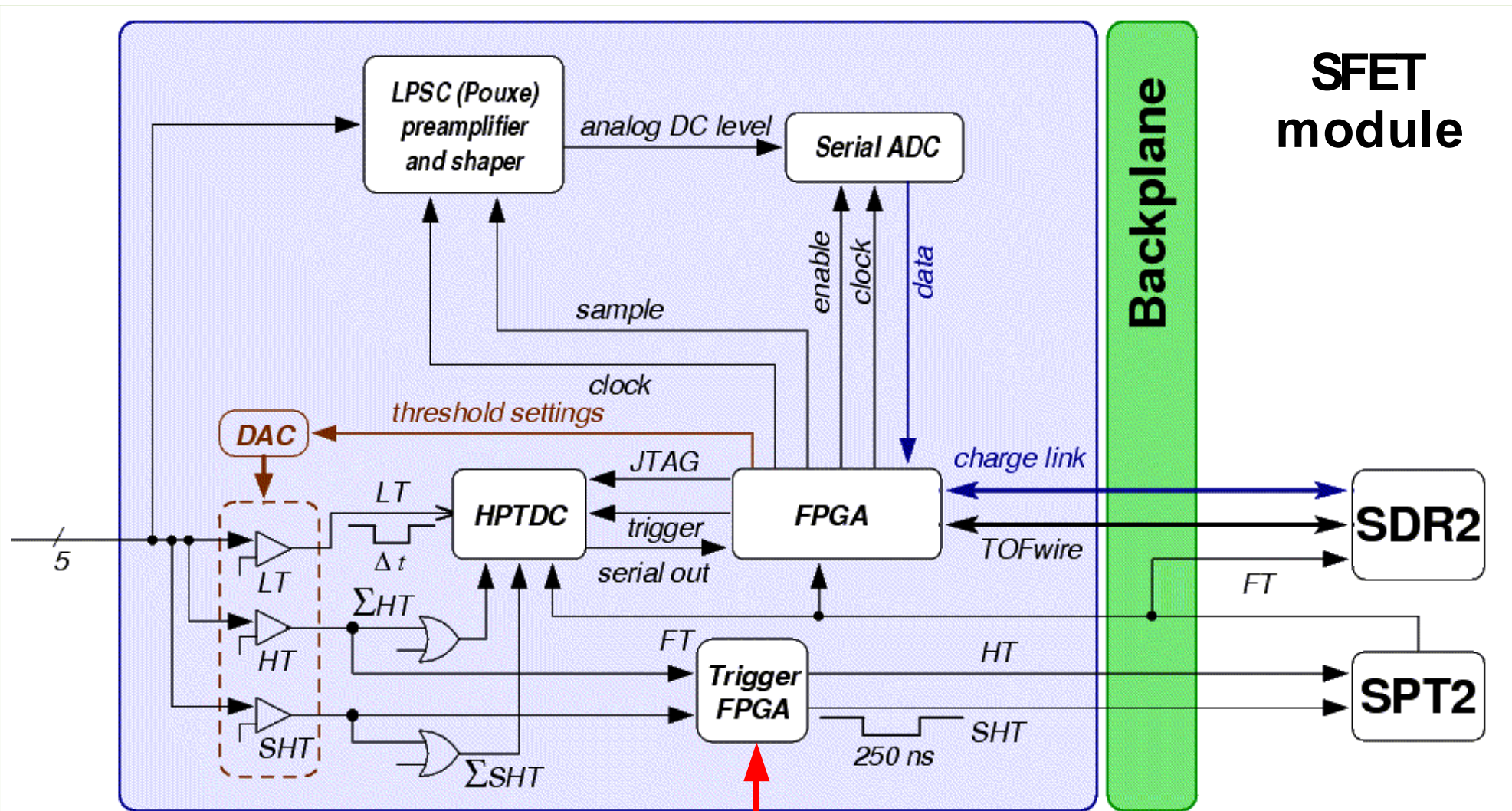
- **Dead time:**

- LT comparators have short (7–8 ns) dead time (output signal width);
- HPTDC inputs have 30 ns default dead time (adjustable);
- HT and SHT comparators have short (7–8 ns) dead time (output signal width);
- HT and SHT output signals have negligible dead time (~1 ns between falling and raising edges);
- HT and SHT output signals are extended if other hits come before their falling edge.

DAQ

- All hits have 1 (optional 2) TDC words: LT (+ sum(HT), optional)
- Very few hits will add sum(SHT)
- (Plus charge words)
- No dead time after FT (no time-exp.): if no LVL1 is generated, there is no additional dead time

New SFET2 scheme



NB. If another hit follows after $t < 250$ ns, the output pulse duration is increased of t .

SFET2 specifications (1)

- **Input signals:**
 - PMT anode (negative pulse): 3-4 ns rise time, 15-20 ns fall time (a bit longer for $Z > 1$ particles)
 - Possible ringing and after-pulse effects
 - Detector double hit resolution ≥ 20 ns
- **Thresholds** (AD8598 dual, AD8564 quad):
 - 3.8 (1.5) ns rise (fall) time, 7-8 ns transit time
 - Timing depends on the input level: previous values are for 100 mV over threshold.
 - HT and SHT directly to SPT2 (no mask)
- **Charge measurement:**
 - Charge integration and sampling sensitive from FT – 6 μ s to FT + 1.7 μ s
 - Single gain (G1); pedestal rms = 1-2 ch.
 - S/N and dynamic range fixed by 1 MIP peak:
1 MIP = 60 (30) ch. \Rightarrow S/N = 30 (15), max = 50 (100) MIP's

SFET2 specifications (2)

- **History:**

- Min. window is $FT - 10 \mu s$ to $FT + 6 \mu s$
- HPTDC internally keeps hits not older than **reject_latency** in level 1 (L1) buffer
- After receiving the **trigger**, HPTDC discards all hits inside the **search_window** (starting at **trigger - trigger_latency**) which do not stay inside the **match_window**
- Times are adjustable within 25 ns

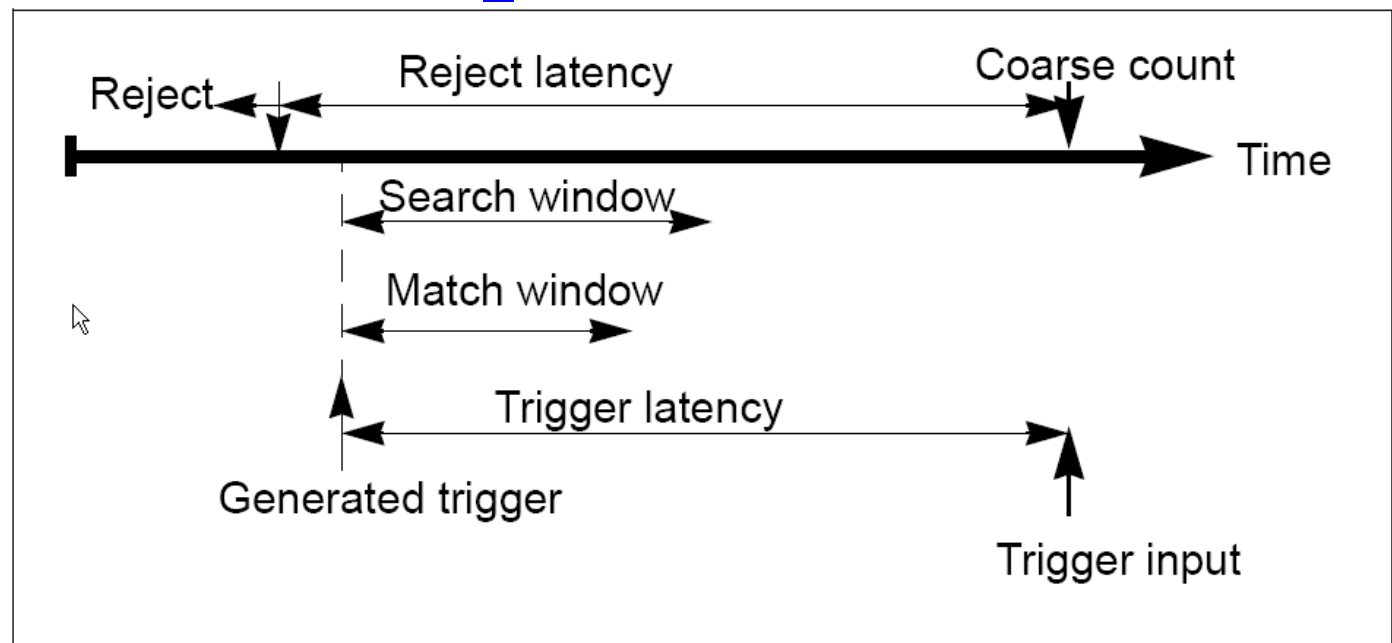


Fig. 8 Trigger, trigger latency and trigger window related to hits on channels

TDC calibrations

- Internal PLL must be initialized at **power-up (10 ms required)** or at periodical resets
- Default values for the RC delay chain will be used, as different corrections seem to be non effective
- External correction table for each TDC, to correct for non-linearity
 - **Off-line correction, if needed**
 - Each SFET2 will be calibrated in lab
 - Calibration runs (and CR data, if possible) in orbit to check tables

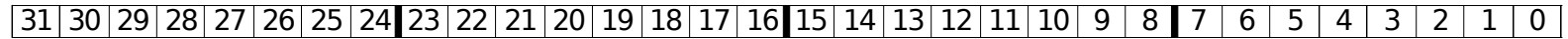
Redundancy

- Logics (i.e. Actel FPGA's) are redundant
- Powering is redundant
- **Thresholds are redundant**
- **Charge measurement is redundant**

Data format

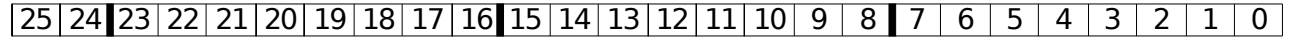
SFET/A: HPTDC internal format

32-bits words (page 24 of hptdc_manual_ver2.2.pdf)



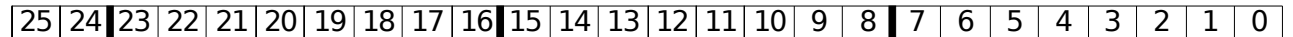
SFET/A: FPGA output time format

26-bits words



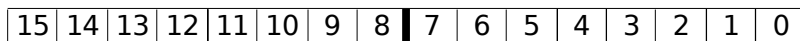
SFET/A: FPGA output temperature format

26-bits words



SDR2: Raw event buffer format

2 consecutive 16-bits words (most significant first)



word0	0	link	FPGA bit 23-12
word1	S	link	FPGA bits 11-0

Example

#	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	temp 15-12	temp0
2	0	0	0	1	temperature bits 11-0											temp1		
															
9	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	temp 15-12	temp0
10	0	1	0	1	temperature bits 11-0											temp1		
11	0	0	0	1	chan	inter.	edge time 18-12									time0		
12	S	0	0	1	edge time 11-0											time1		
															
19	0	1	0	1	chan	inter.	edge time 18-12									time0		

board	link	hex
SFET2a	0 0 1	0x1
SFET2b	0 1 0	0x2
SFET2c	0 1 1	0x3
SFET2d	1 0 0	0x4
SFEA2	1 0 1	0x5

Open issues

- Dead time TDC input: default 30 ns (5, 10, 100 ns are possible). **Fixed** or adjustable?
- Delay between FT and TDC_trigger: **fixed** or adjustable? Value(s)?
- History depth: fixed or adjustable? Value(s)?
 - If history adjustable, match_window and trigger_latency will be adjusted by the same amount.
- Status register of HPTDC: when to be checked? what to do in case of problems?
- Initialization of PLL must be done at power-up and in case of problems: via DSP (on SDR2)? via slow-control?
- Threshold duration for double pulses: how long?