AMS Internal Note
ScintEle–05 v3.4

AMS-02 scintillators data acquisition specifications

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ABSTRACT

Specifications for AMS-02 data acquisition scintillator electronics. Guide/check-list for the developers. **DRAFT!**

Contents

1. Document history

Changes from previous version are in red.

Changes since version 3.2 (21 Sep 2006)

- Changed figure 1.
- Changed SFET2/SFEA2 data format.
- Changed the section order.
- Added end-of-record to raw event buffer.

2. Preliminary notes

1. Normal event: one fast trigger (FT) is followed by one level-1 trigger (LVL1) signal, after 1.0 ± 0.1 μs.
2. Scintillator front-end (SFE) electronics start operating with the FT, but
3. data collection starts with the LVL1. During data collection the system is busy (no trigger will be generated).
4. Special treatment is needed when FT is not followed by the LVL1.
5. SFE electronics are distributed into the following units:
   (a) SFET2 (redundant, inside S-crate): TOF time & charge measurement
   (b) SFEA2 (redundant, inside S-crate): ACC time & charge measurement
   (c) SFEC (not redundant, inside TOF): TOF charge measurement
   (d) SPT2 (redundant, inside S-crate, pre-trigger): trigger patterns, scalers
6. SFE data collection is performed by the SDR2 board (redundant, inside S-crate).
7. FT distribution:
   (a) SPT2 receives 2 sets of 4 FT signals each, from the trigger units (JLV1A and JlLV1B).
   (b) Only one set is active, in normal conditions.
   (c) SPT2 logically adds these signals, producing a double output (for redundancy), and
   (d) provides the result to SDR2, SFET2 and SFEA2 boards.
   (e) SDR2, SFET2, SFEA2 must use the logical sum of the two FT inputs.
   (f) Each SDR2, SFET2, SFEA2 board has dedicated input lines for the FT (point-to-point redundant connections with SPT2).
   (g) On backplane, FT is a active-high TTL3.3V signal.
8. LVL1 distribution:
   (a) SDR2 receives 2 LVL1 signals from JLV1A/JLV1B.
   (b) Only one signal is active, in normal conditions.
   (c) SDR2 logically adds the two signals producing a double output (for redundancy), and
   (d) provides the result to SFET2 and SFEA2 boards.
   (e) SFET2 and SFEA2 boards must use the logical sum of the two LVL1.
   (f) LVL1 is sent as a bus: all SFET2/SFEA2 boards use the same two lines.
   (g) On backplane, LVL1 is a active-high TTL3.3V signal.
9. Event data consist of charge, time, trigger patterns, temperature.
10. Charge data follow separate links from those carrying time, trigger and temperature data.
11. Each board provides:
    (a) SFET2 - charge; temperature + time;
    (b) SFEA2 - charge; temperature + time; identical to SFET2 format.

(c) SPT2 - trigger patterns;
(d) SFEC - charge (via SPT2).

12. Charge data collection starts with LVL1 and has critical timing.
13. Charge data collection is driven by SDR2, which takes care of the timing.
14. Time (+ temperature) data collection starts not earlier than 6.5 μs after FT, if LVL1 has arrived.
15. Trigger data collection may start immediately after LVL1.
16. If the FT is not followed by the LVL1:

    (a) charge data collection does not start;
    (b) time data collection does not start. SFET2 and SFEA2 boards may have 1-2 μs dead time. **[TO BE CHECKED WITH THE PROTOTYPE]**;
    (c) trigger data collection does not start;

FIX ME!

17. After a FT, SDR2 enables its BUSY output, which will veto FT generation (but not LVL1 generation).
18. BUSY will stay active for at least 1.5 μs after a FT (maximum allowed delay for LVL1 to come to SDR2).
19. SDR2 structure:

    (a) (backplane) links to SPT2 and the SFE boards originate from the A.FE Actel FPGA;
    (b) these are serial links whose speed cannot exceed (1 bit)/(80 ns);
    (c) (front-panel) links to the rest of the system (AMSwire, LVL1 and BUSY) are connected to the A.CDP Actel FPGA;
    (d) event data collected by a.FE are transferred to A.CDP (which sends them to the raw event buffer) via a 16-lines parallel bus,
    (e) whose transfer rate cannot exceed (1 word)/(60 ns). In practice, the maximum bus speed is roughly (1 word)/(100 ns) on the average.

20. Charge data collection procedure:

    (a) SDR2 sends strobes on "charge control" links, which are the "clocks" of the remote units;
    (b) remote units are state machines whose transitions are driven by the aforementioned lines;
    (c) operations are logically divided into 3 phases:
        i. clean-up of memory effects: few transitions to be completed within 0.5 μs after the FT. *Done only by SFET2 and SFEA2* (without SDR2 strobes on the charge control link);
        ii. sample & hold of the analog signals: to be made 0.7 ± 0.1 μs after the LVL1. Driven by SDR2. Timing is important;
        iii. digitization and data transfer to SDR2: relatively long sequence (< 35 μs) whose timing is not crytical. The only constraint is the time-out (3 μs) of the

remote unit: this is the maximum delay between two transitions of the input charge control line before a self-clear is made.

21. All words transmitted by A.FE to A.CDP will be sequentially put into one of the 4 ”raw event buffers” (starting at different addresses on the main SDR2 memory).
22. Because A.FE sends a variable amount of data to A.CDP, **[A SPECIAL MARKER IS USED TO FLAG THE END OF THE RAW EVENT BUFFER]**. This flag is a null 16-bit words (i.e. 16 zeroes). **FIX ME!**
23. In the ”raw mode”, the DSP will insert the raw event buffer, **[FROM ITS FIRST WORD (INCLUDED) TO THE END MARKER (EXCLUDED)]**, into the data section of the output event buffer. Then this buffer will be sent to a JINJ via AMSwire when requested. **FIX ME!**
24. In the ”compressed mode” DSP will perform operations **[TO BE DEFINED]**. **FIX ME!**

3. Front-end data format

3.1. Charge

1. Charge words (serially) coming from SFE boards are 12-bits long, MSB first.
2. A.FE prepend the link address to each charge word, i.e. the link address is encoded in the 4 most significant bits of each charge word.
3. Channel is not encoded in the raw event buffer charge data: it can be found from the word offset.

3.2. Trigger patterns

Note. The system is not to be used with both power lines (28 V) turned on. However, in case of necessity, it should be able to operate this way. This can happen if there are few dead channels in side A of some board and other dead channels in side B of some other board. In this case, one might turn on both 28 V lines and turn off side A of part of the crate and side B of the rest of the crate.

The only exception are SPT2 and SDR2. HT and SHT logic signals coming out from side A (B) of all SFET2s are received by side A (B) of SPT2. But SPT2 has to make the (masked) OR of sets of signals coming from different boards, hence inside SPT2 A and B halves must communicate in some way. In the same way, data coming from side A (B) of SFET2 and SFEA2 boards are sent only to side A (B) of SDR2. Hence, SDR2 must have both halves working, in order to send data to the higher level (JINJ boards), where they will be assembled into events.

The design choice (see also figure 1) was the following:

Side A (B) FPGA:

1. CP,0 = p0_out = (masked) OR of first half plane HT + p0_in;
2. CP,1 = p1_out = (masked) OR of second half plane HT + p1_in;
3. CT,0 = t0_out = (masked) OR of first half plane HT + t0_in;

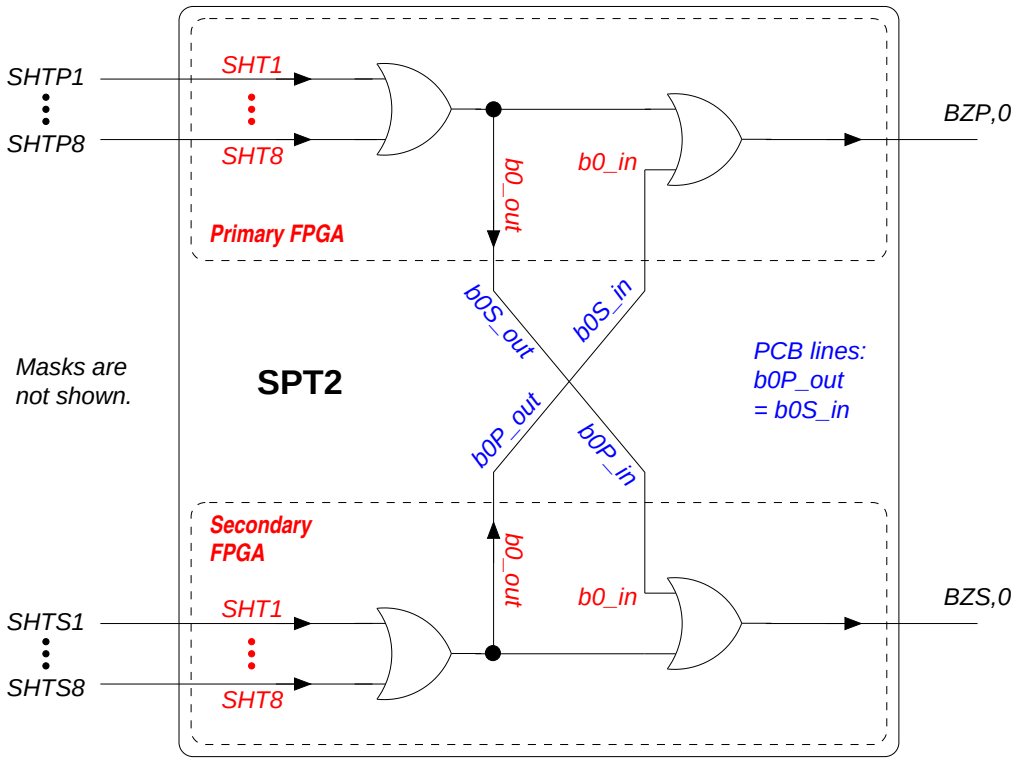

Figure 1. Example of pre-trigger logics inside SPT2. Leftmost names refer to backplane lines; rightmost names refer to front-panel lines; red names refer to VHDL, which is the same in both FPGAs; blue names are PCB lines. Input lines can be masked out (not shown).

4. CT,1 = t1_out = (masked) OR of second half plane HT + t1_in;
5. BZ,0 = b0_out = (masked) OR of first half plane SHT + b0_in;
6. BZ,1 = b1_out = (masked) OR of second half plane SHT + b1_in;

where

- CP,*i*, CT,*i* and BZ,*i* are sent to JLV1*;
- p*i*_out, t*i*_out, and b*i*_out are sent to the FPGA on the other side;
- p*i*_in, t*i*_in, and b*i*_in are received by the FPGA on the other side.

7. p*i*_in, t*i*_in, and b*i*_in patterns are saved together with single-channel patterns at each FT.
8. SPT2 sends the 18 + 18 = 36 bits of the two trigger patterns encoding them into 4 16-bits words, which are sent to the raw event buffer in the same order (word_0 to word_3) they are received (figure 2):

   (a) HT trigger patterns (18 bits: “h17”–”h0”) and 4 signals coming from the other side FPGA (CP bits: “p1”, “p0”; CT bits: “t1”, “t0”) are encoded in the first two SDR2 words (lowest 11 bits of word_0 and word_1);

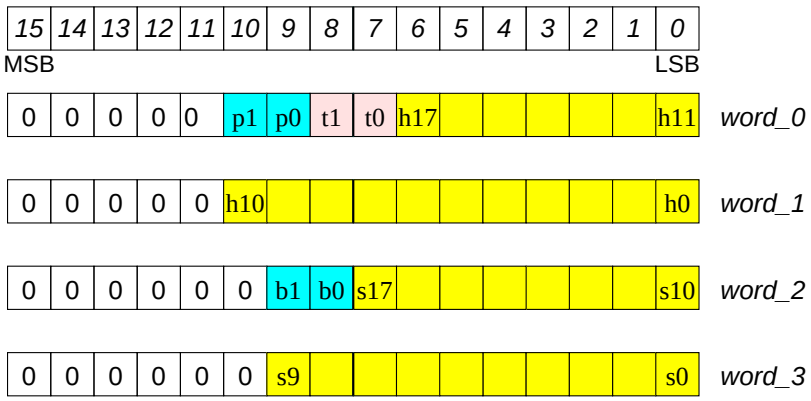

Figure 2. Output SPT2 data format. Serial transmission is MSB to LSB, word_0 to word_1.

(b) SHT trigger patterns (18 bits: "s17"–"s0") and 2 signals coming from the other side FPGA (BZ bits: "b1", "b0") are encoded in the first two SDR2 words (lowest 10 bits of word_0 and word_1).

3.3. Time and temperature

1. Temperature words (serially) coming from SFET2 and SFEA2 boards are 26-bits long, MSB first (figure 3).
   (a) The first bit (bit 25) is the "stop" bit: $S = 1$ for the last word coming from the considered link;
   (b) the second bit (bit 24) is the "parity" bit P: the total number of bits equal to 1 (including P itself) must be *even*[1].
2. Time words from SFET2 and SFEA2 boards format (figure 3):

[1]Hence $P = \sum_{i \neq 24} b_i \mod 2$, where b_i are the word bits.

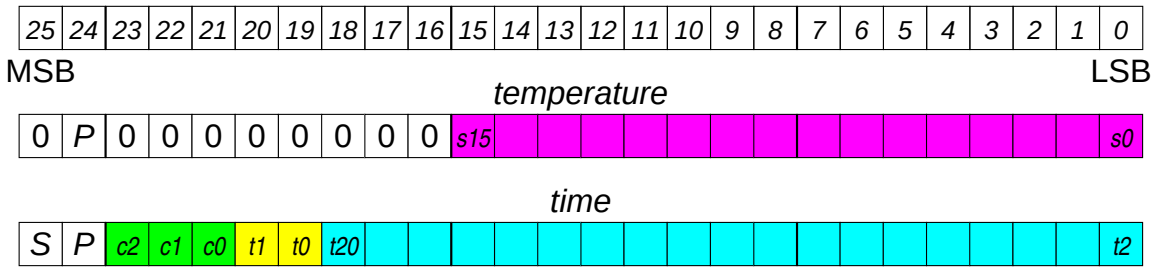

Figure 3. Output SFET2 data format. Serial transmission is MSB to LSB. The first bit S is the "stop" bit: $S = 1$ for the last word. It is followed by the parity bit: $P = 1$ or 0 in order to have an *even number* of '1's in the word (including P itself). Then there is the channel address (MSB first) and the time word.

(a) bits 23-21 encode the TDC channel, most significant bit first:

TDC ch.	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7
Input	Ch1	Ch2	Ch3	Ch4	Ch5	FT	aux1	aux2

(b) the following 21 bits encode the time, most ("t20") to least ("t0" significant bit, preceded by the least 2 bits (called "interpolated time" in HPTDC manual).

4. Front-end data collection specifications

1. When FT reaches SDR2, the latter must activate the BUSY and wait for the LVL1.
2. If no LVL1 is received, 1.5 μs after FT the data collection procedure is aborted (just before sending the strobe which enters phase 20(c)ii of charge read-out, §2 on page 4). In this case:
   (a) SDR2 has no wait:
   (b) A.FE is reset and
   (c) the BUSY is disabled.
3. From now on, we suppose that a LVL1 signal followed the FT. A.FE starts phase 20(c)ii of charge read-out, 0.7 μs after LVL1 (i.e. 1.7 μs after FT, i.e. 0.2 μs after the time-out of the previous item).
4. At this point, slow control commands may be executed in parallel with the charge data collection (because they follow separate links).
5. The amount of charge data is fixed: 9 links × 10 channels = 90 words, 16-bits each.
6. After having transferred all charge words to A.CDP, A.FE will collect and transfer
   (a) trigger patterns from SPT2 (4 words), then
   (b) temperature + time words from SFET2 and SFEA2 boards (at least 5 temperature words plus 5 FT time words).
7. In case a slow control command is being executed, previous step is delayed.
8. In this case, the A.CDP keeps the BUSY enabled. BUSY will be active until the end of data collection from A.FE.
9. **[IF NO TIME-OUT IS SET ON SLOW-CONTROL COMMAND EXECUTION, SDR2 COULD FREEZE]** **FIX ME!**
10. Trigger patterns are written to the raw event buffer immediately after charge words. Because their number is fixed, the position in the buffer identifies the origin.
11. A.FE collects data in parallel from SFE boards. When the input buffers of the backplane links contain one charge word each, these words are sent to A.CDP.
12. The order in which these words are sent to A.CDP is:
    (a) SFET2a
    (b) SFET2b
    (c) SFET2c
    (d) SFET2d
    (e) SFEA2

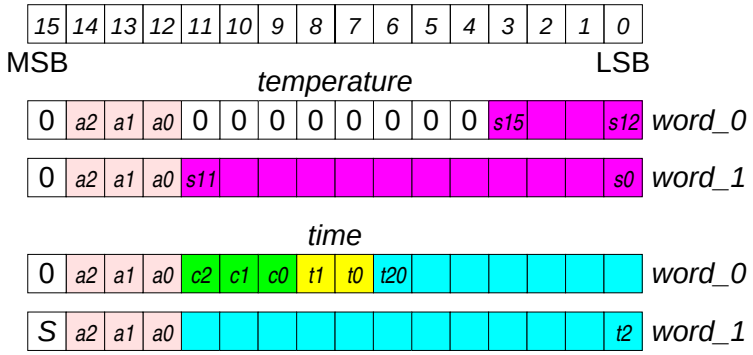

Figure 4. Raw event buffer: structure of temperature and time data. Bits "a2 a1 a0" encode the link number, MSB first.

(f) SFEC1a
(g) SFEC1b
(h) SFEC2a
(i) SFEC2b

13. Trigger patterns are followed by temperature and time words from SFET2 and SFEA2 boards.
14. The SFET2 and SFEA2 words are 26-bits long (figure 3).
    (a) the first (i.e. most significant) bit is the "stop" bit S: $S = 1$ for the last word coming from a given board;
    (b) the second bit is the "parity" bit P: the total number of bits equal to 1 (including P itself) must be *even*.
15. SFET2 and SFEA2 words will be split into two adjacent 16-bits words (word_0, word_) when transferred to A.CDP:
    (a) the second bit of the 26-bits word is discarded (the parity is checked by A.FE[2]);
    (b) the last (lowest) 24 bits are split into 12 + 12 bits, and
    (c) the first (i.e. most significant) 12 bits are encoded into the last 12 bits of the first SDR2 16-bits word (word_0),
    (d) the last (i.e. least significant) 12 bits are encoded into the last 12 bits of the second SDR2 16-bits word (word_1);
    (e) the stop bit is mapped into the first bit of word_1 only;
    (f) the following 3 bits (bit 14 to bit 12) of both word_0 and word_1 encode the link number, most to least significant bit;
    (g) links are numbered as follows:

Link	0x1	0x2	0x3	0x4	0x5
Board	SFET2a	SFET2b	SFET2c	SFET2d	SFEA2

[2]The parity error is $E = \sum_{i=0..25} b_i \mod 2$ (the sum runs over *all* bits).

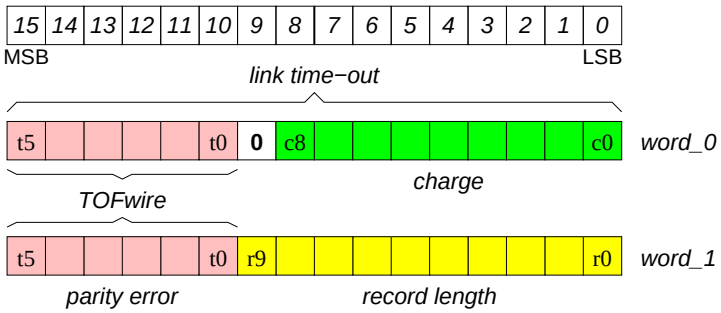

Figure 5. Raw event buffer: structure of the end-of-record words.

16. The first word coming out from a SFET2/SFEA2 encodes the temperature.
17. The temperature is encoded in the last 16 bits of this 26-bit word.
18. The temperature word is split into 2 × 16-bits words (word_0, word_1) in the SDR2 raw event buffer:
    (a) the 4 most significant bits of the temperature word (i.e. bits 15-12) are mapped into the last (lowest) 4 bits of word_0;
    (b) the last (lowest 12 bits of the temperature word (i.e. bits 11-0 are mapped into the last (lowest) 12 bits of word_1.
19. The raw event buffer memory layout will be:
    (SFET2a,ch.1), (SFET2b,ch.1), (SFET2c,ch.1), (SFET2d,ch.1), (SFEA2,ch.1), (SFEC1a,ch.1), (SFEC1b,ch.1), (SFEC2a,ch.1), (SFEC2b,ch.1), (SFET2a,ch.2), (SFET2b,ch.2), (SFET2c,ch.2), (SFET2d,ch.2), (SFEA2,ch.2), (SFEC1a,ch.2),
    ... all charge words, until (SFEC2b,ch.10)), then
    (SPT2,word1), (SPT2,word2), (SPT2,word3), (SPT2,word4),
    followed by:
    (a) double temperature words
    (SFET2a,Temp1), (SFET2a,Temp2), (SFET2b,Temp1), (SFET2b,Temp2), (SFET2c,Temp1), (SFET2c,Temp2), (SFET2d,Temp1), (SFET2d,Temp2), (SFEA2,Temp1), (SFEA2,Temp2)
    (b) PLUS 2 time words per link (usually the FT time)
    (SFET2a,FT-a), (SFET2a,FT-b), (SFET2b,FT-a), (SFET2b,FT-b), (SFET2c,FT-a), (SFET2c,FT-b), (SFET2d,FT-a), (SFET2d,FT-b), (SFEA2,FT-a), (SFEA2,FT-b)
    (c) AND zero or more pairs of time words
    (SFET2*,ch?a), (SFET2*,ch?b),...
20. At the end of the raw event buffer there should be the following words (see figure 5):
    (a) the one-to-last word (word_0) contains the status of every link tim-out, with
        i. TOFwire links mapped on the 6 most significant bits, with sequence (SFET2a to SFET2d, SFEA2, SPT2);

ii. charge links mapped on the 9 least significant bits, with sequence (SFET2a to SFET2d, SFEA2, SFEC1a, SFEC1b, SFEC2a, SFEC2b);

(b) the last word (word_1) contains the parity error of each TOFwire link (6 most significant bits, same sequence as before), and

(c) the current record length (number of 16-bits words, including the last one), mapped on the lowest 10 bits.