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EDR and ETRG MAPS

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1 ECAL boards

There are 2 E-CRATES each one is composed by 11 boards (See table 1):

- **6 EDRs** (ECAL data reduction)
- **3 EPSFE** (Slow Control for front end)
- **1 JINF** (DAQ node)
- **1 ETRG** (Trigger board for 1 view, X or Y)

SLOT#	1	2	3	4	5	6	7	8	9	10	11
BOARD	EDR	EPSFE	EDR	EDR	EPSFE	EDR	JINF	EDR	EPSFE	EDR	ETRG
#	0	0	1	2	1	3	-	4	2	5	-

Table 1: Boards in 1 ECAL crate.

Each board is redundant (part A and B), the slave addresses for DAQ boards that appear in the node status in the JINF event fragment are shown in table 2.

	EDR						ETRG
	0	1	2	3	4	5	
PART A	00	04	08	0c	10	14	16
PART B	01	05	09	0d	11	15	17

Table 2: EDR and ETRG Boards address (in hexadecimal) in DAQ event.

2 EDR

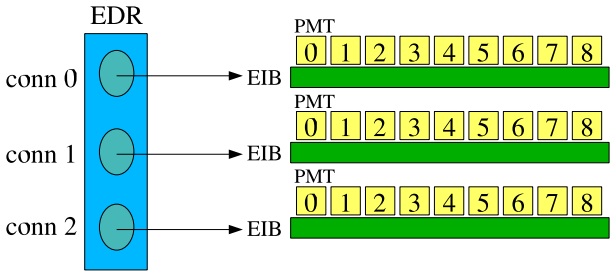

Figure 1: EDR multiplicity.

Each EDR (fig. 1) reads 3 EIBs. Each EIB reads a line of 9 PMTs. Each PMT has 9 channels: 4 anodes with low gain, the same 4 anodes with high gain and the dynode.

The format of the EDR raw event (243 channels) is shown in table 3.

PMT CHANNEL	description	CONN	PMT					ADC address			
0	ANODE 0 low	2	8	7	..	0	→	0	1	..	8
		1	8	7	..	0	→			..	17
		0	8	7	..	0	→			..	26
1	ANODE 0 high	2	8	7	..	0	→			..	35
		1	8	7	..	0	→			..	44
		0	8	7	..	0	→			..	53
2	ANODE 1 low	2	8	7	..	0	→			..	62
		1	8	7	..	0	→			..	71
		0	8	7	..	0	→			..	80
3	ANODE 1 high	2	8	7	..	0	→			..	89
		1	8	7	..	0	→			..	98
		0	8	7	..	0	→			..	107
4	ANODE 2 low	2	8	7	..	0	→			..	116
		1	8	7	..	0	→			..	125
		0	8	7	..	0	→			..	134
5	ANODE 2 high	2	8	7	..	0	→			..	143
		1	8	7	..	0	→			..	152
		0	8	7	..	0	→			..	161
6	ANODE 3 low	2	8	7	..	0	→			..	170
		1	8	7	..	0	→			..	179
		0	8	7	..	0	→			..	188
7	ANODE 3 high	2	8	7	..	0	→			..	197
		1	8	7	..	0	→			..	206
		0	8	7	..	0	→			..	215
8	DYNODE	2	8	7	..	0	→			..	224
		1	8	7	..	0	→			..	233
		0	8	7	..	0	→			..	242

Table 3: EDR RAW event format and adc channel addresses.

The compressed event has an ADC address before the adc value that goes from 0 to 242; this must be converted into EDR CONNECTOR ($\rightarrow EIB$), PMT NUMBER and PMT CHANNEL using table 3.

3 From hardware address to position

The calorimeter grid can be defined using as granularity 1 PMT or 1 ANODE:

- **1 PMT grid:** 9 Superlayers × 36 Columns
- **1 ANODE grid:** 18 Layers × 72 Cells

3.1 Superlayers

The 4 calorimeter faces are defined in fig. 2.

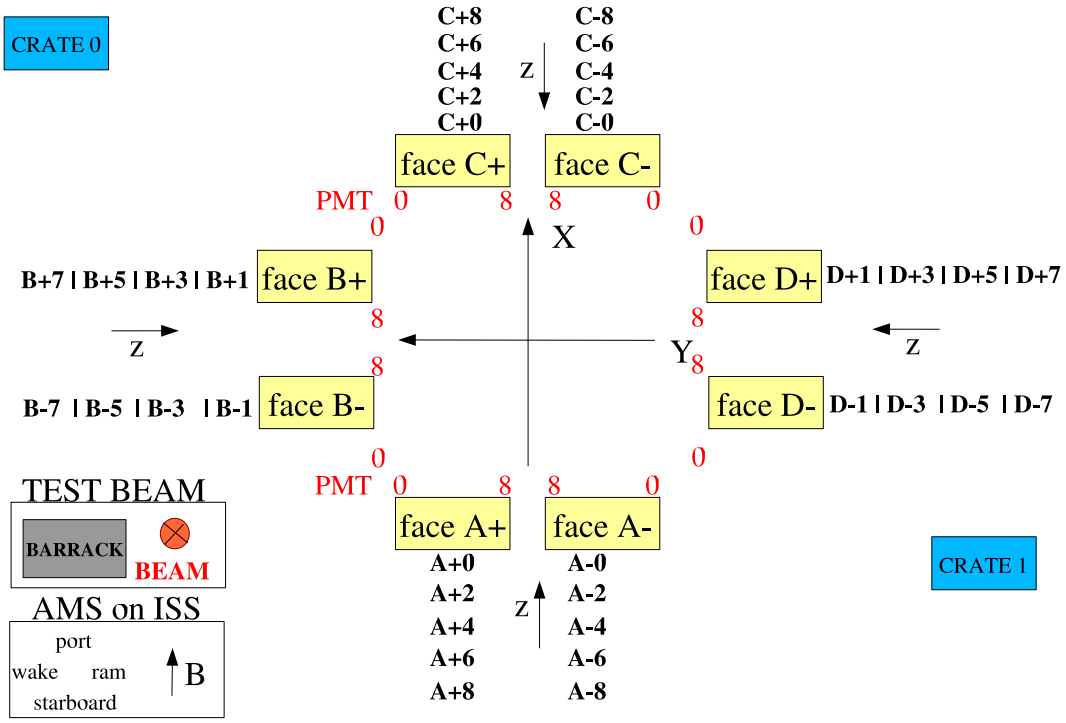

Figure 2: Face and EIB names.

Faces A and C read the Y coordinate and have 5 superlayers.

Faces B and D read the X coordinate and have 4 superlayers.

The top superlayer, the one closest to the beam (in AMS the one close to the RICH) is superlayer 0 and has PMTs reading the Y coordinate (bending direction). The following superlayer, number 1, has PMTs reading the X coordinate.

Each face has 18 PMTs. Since each EIB reads out 9 PMTs, there are 2 EIBs per superlayer per face. The EIBs are then named using the face name (A,B,C,D), the face side (+ or - for positive or negative x or y) and the superlayer number (see fig.2).

3.2 Columns

Along one coordinate the PMT columns are alternated between the two opposite faces (fig.3): column 0 is the one at most negative X or Y that is on face A for Y and on face B for X.

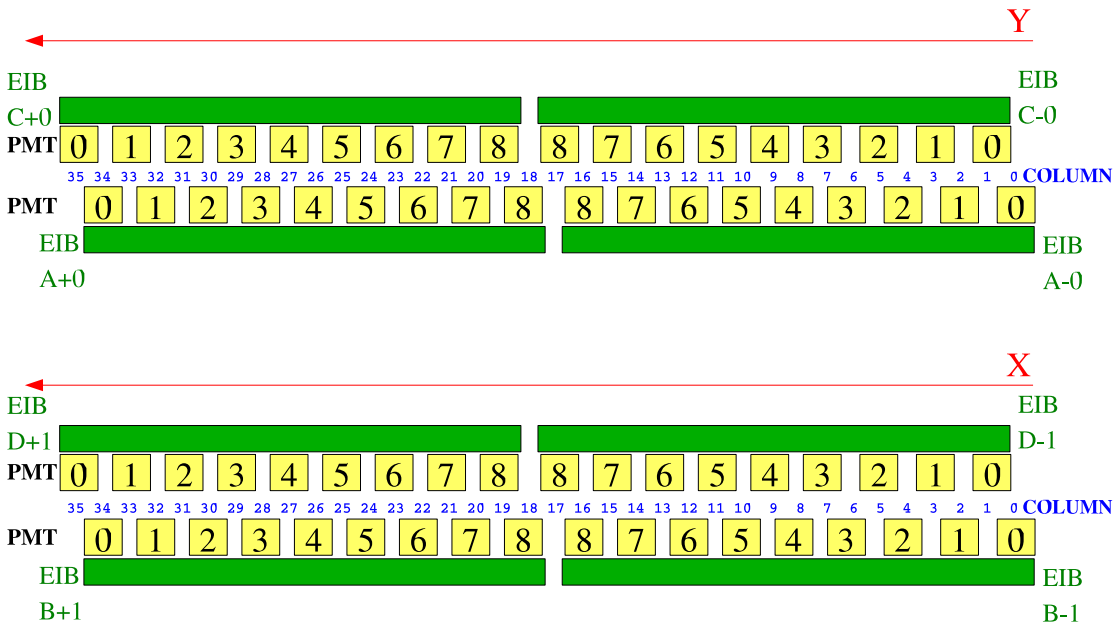

Figure 3: Column numbering scheme.

Following the PMT number definition of the EDR raw format (table 3), PMT 8 is always in the middle of calorimeter, PMT 0 is always at calorimeter edge: e.g., PMTs 0 of EIBs on face A- are on column 0, while PMTs 0 of EIBs on face A+ are on column 34.

3.3 Layers and Cells

Table 4 shows how the 4 anodes are numbered within the PMT as seen standing in front of a calorimeter face.

	left	right
top	3	2
bottom	0	1

Table 4: Anode numeration inside a PMT looking at the calorimeter face.

All PMTs have been mounted in the same way. This implies a specularity between the opposite faces (fig.4) when converting the COLUMN and ANODE number in a cell number:

$$face\ A\ and\ B:$$

$$cell = \quad Column * 2 \quad (\ anode\ 1\ and\ 2\ )$$

$$cell = \quad Column * 2 + 1 \quad (\ anode\ 0\ and\ 3\ )$$

$$face\ C\ and\ D:$$

$$cell = \quad Column * 2 \quad (\ anode\ 0\ and\ 3\ )$$

$$cell = \quad Column * 2 + 1 \quad (\ anode\ 1\ and\ 2\ )$$

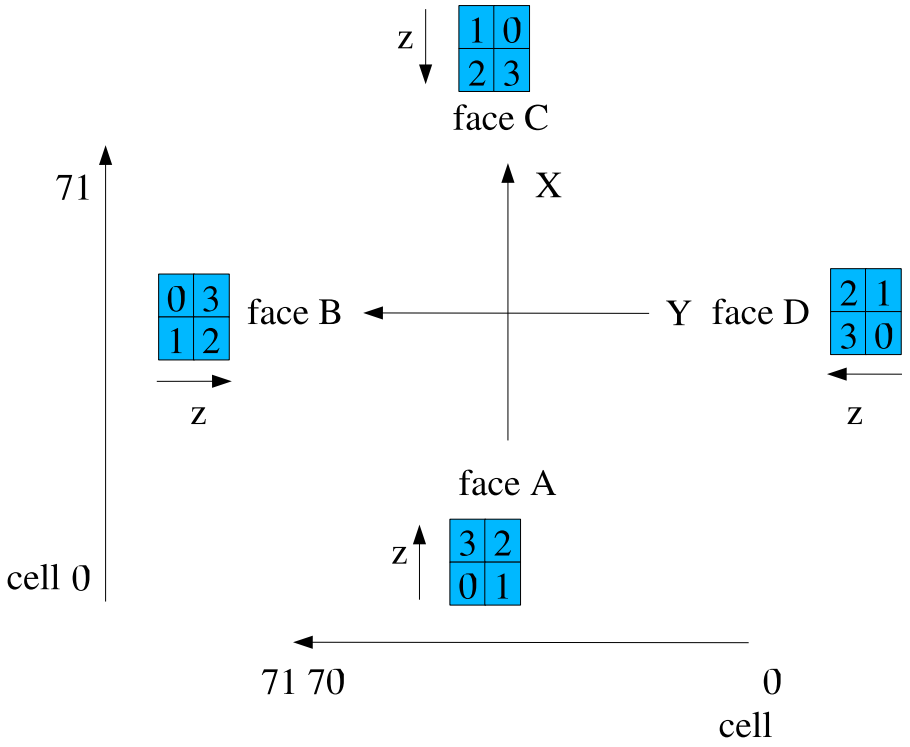

Figure 4: Anodes numeration versus x and y.

The top layers, the closest to the beam (in AMS the closest to the RICH), are layers 0 and 1, with PMTs reading the X coordinate. The following layers, number 2 and 3, read the Y coordinate.

For all the faces the layer number is given by:

$$layer = \quad Superlayer * 2 + 1 \quad (\ anode\ 0\ and\ 1\ )$$

$$layer = \quad Superlayer * 2 \quad (\ anode\ 2\ and\ 3\ )$$

4 EDR-EIB cabling

The EIB-EDR cabling used in the test beam is reported in table 5.

JINF 0	EDR					
CONNECTOR	0	1	2	3	4	5
0	B+1	B-1	B+3	B-3	B+5	B-5
1	A+0	C+0	A+8	C+8	B-7	B+7
2	C+2	A+2	C+4	A+4	C+6	A+6
JINF 1	EDR					
CONNECTOR	0	1	2	3	4	5
0	D-1	D+1	D-3	D+3	D-5	D+5
1	C-0	A-0	C-8	A-8	D+7	D-7
2	A-2	C-2	A-4	C-4	A-6	C-6

Table 5: EIB cabling on EDR connectors.

In this way each EDR serves 2 trigger EIBs (Superlayers from 1 to 6) and 1 non-trigger EIB, always on connector 1 (Superlayers 0, 7 and 8).

4.1 Examples of conversion

HARDWARE ADDRESS								PMT GRID		ANODE GRID	
JINF	EDR	CONN	PMT	CHAN	anode	gain	EIB	superl	col	lay	cell
1	1	1	0	1	0	high	A-0	0	0	1	1
1	1	1	0	3	1	high	A-0	0	0	1	0
1	1	1	0	5	2	high	A-0	0	0	0	0
1	1	1	0	7	3	high	A-0	0	0	0	1
0	3	1	0	3	1	high	C+8	8	35	17	71
0	3	1	0	5	2	high	C+8	8	35	16	71
0	1	0	0	1	0	high	B-1	1	0	1	1
0	1	0	0	3	1	high	B-1	1	0	1	0
0	1	0	0	5	2	high	B-1	1	0	0	0
1	1	1	0	7	3	high	B-1	1	0	0	1
1	4	1	0	3	1	high	D+7	7	35	15	71
1	4	1	0	5	2	high	D+7	7	35	14	71

Table 6: Examples of conversion from EDR address (jinf, edr, connector, pmt number, pmt channel) to the position in the calorimeter: (superlayer, column) or (layer, cell).

5 ETRG

The ETRG board performs the ECAL trigger algorithm. This algorithm is based on the PMT dynode information: inside the EIB the dynode signal is compared with a given threshold and then a bit is set to 1 if the threshold is passed (0 otherwise).

Only the PMTs of the central part of the calorimeter are used (Superlayers from 1 to 6).

There are 2 ETRGs, one for each view (X and Y). Each ETRG board produces one ECAL Fast Trigger signal (XF or YF) and one ECAL Level 1 Trigger signal (XA or YA). The ETRG inserted in E-CRATE 0 is connected with the EIBs on face B and D (X view), the one in crate 1 is connected to EIBs on face A and C (Y view).

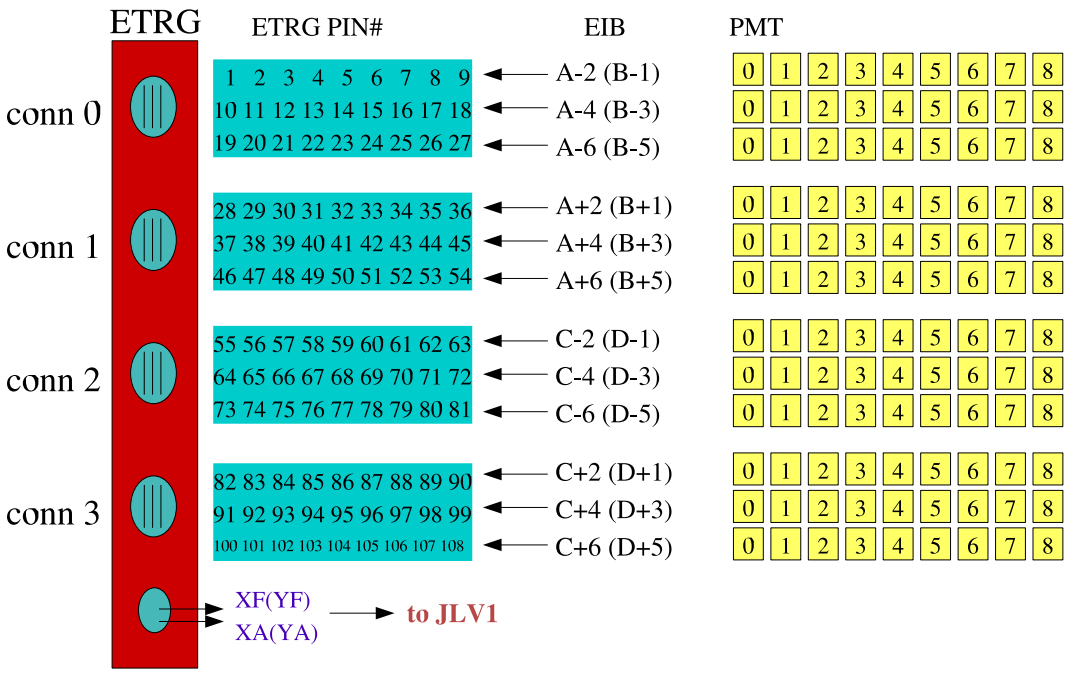

Figure 5: ETRG connections to PMTs.

Each ETRG has 5 connectors (fig.5): 4 input connectors receiving the bits from 108 PMT dynodes and 1 output connector sending the trigger signals to the JLV1 board.

Each input connector has 27 pins cabled to 3 EIBs belonging to the same half face. The first line corresponds to the EIB on the top (the one closest to the RICH).

5.1 ETRG data format

Each ETRG sends to its JINF (via the back plane) the 108 input bits and the ECAL Fast and Level 1 trigger bits.

The 108 dynode bits are **sorted** by ETRG by Superlayer and Column: first bit corre-

sponds to column 0 of the top superlayer, last bit corresponds to colum 35 of the bottom superlayer.

Nonetheless, since the daq protocol requires only 16 bits word, the ETRG information is split in 7 words of 16 bits. In each 16 word the bit order is **reversed** so that the less significative bit corresponds to the lowest ETRG bit. XF(YF) and XA(YA) bits are the most significative of the 7^{th} word (fig. 6). The third and fourth MSB of the 7^{th} word are currently unused.

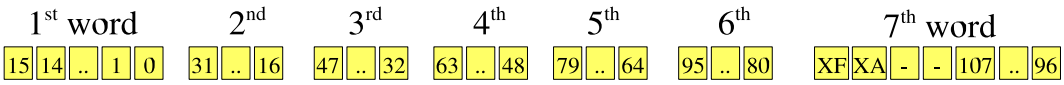

Figure 6: ETRG event fragment.

5.2 Example of conversion

Trigger word:

3c00 5002 4006 3aed 3e4 cec4

corresponds to:

```
  PMT  0  1  2  3  4  5  6  7  8  9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35
(SL1)  0  0  0  0  0  0  0  0  0  0  1  1  1  1  0  0  0  1  0  1  1  0  0  1  0  1  0  0  0  0  0  0  0  0  0  0
(SL3)  0  0  0  0  0  0  0  0  0  0  1  0  0  1  0  1  1  1  1  1  1  0  1  1  0  1  0  0  0  0  0  0  0  0  0  0
(SL5)  0  0  0  0  0  0  0  0  0  0  1  0  0  1  1  1  1  1  1  1  1  0  1  1  0  0  0  1  0  0  0  0  0  0  0  0
```

Looking at the 2 MSB of the seventh word one sees that XF=1 and XA=1.