

EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH

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Slow control S9011AT and TPSFE boards

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Abstract

This document describes the VHDL code written for the slow control in the Tracker electronics. Functionalities are reported and the architecture of the system is shown in a schematic format.

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1 Description of the VHDL code for the S9011AT board

There are 2 LeCroy-slave units communicating with the T-crate, where JINF board is the master.

The 2 LeCroy units read or write data from/to registers using the “COM_BUS” 16 bit communication bus; to avoid possible conflicts, it has been needed an arbiter (CU_W_R_A_B) for the management of the access to the “COM_BUS”. The LeCroy_A unit has the priority on the LeCroy_B unit.

The bus is occupied only 1 cycle @ 4MHz (MASTER_CLK) for W/R operations; this is possible thanks to the VALID_DATA_TX signal, a pulse during 1 cycle of clock @ 4 MHz. It is generated at the falling edge of the DATA_CLK LeCroy communication signal (see PULSE_GEN module).

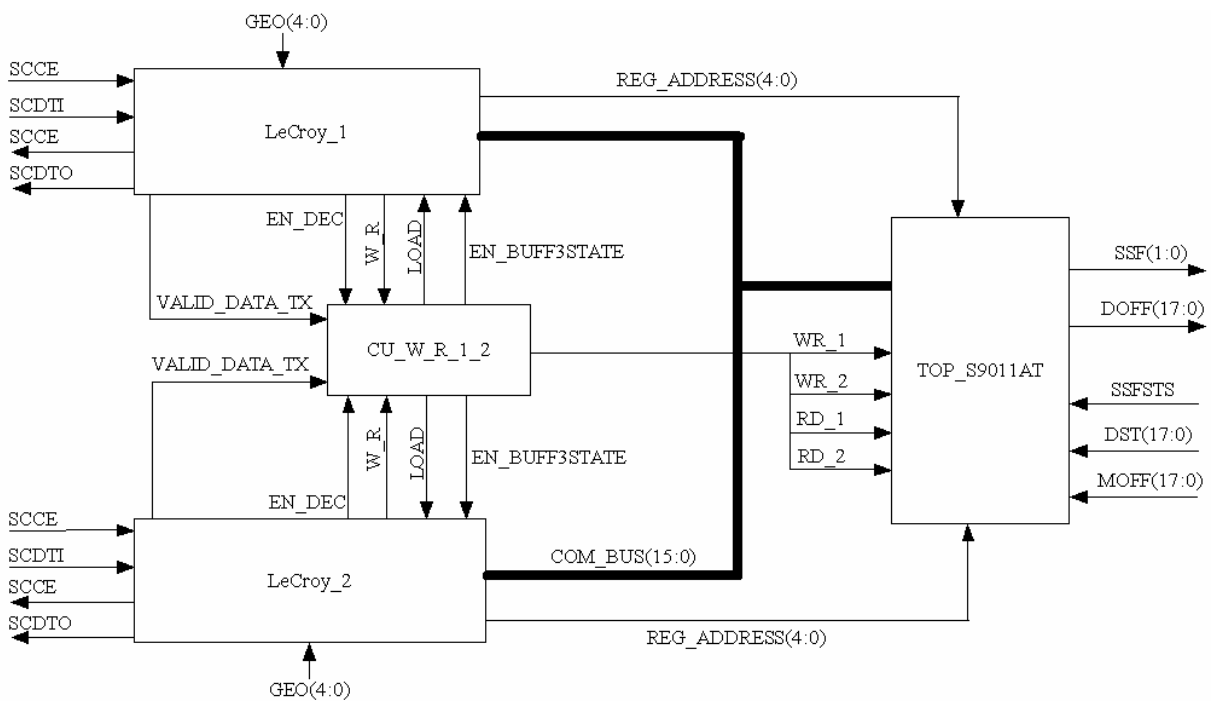


Figure 1

Top-level of the S9011AT's FPGA

1.1 LeCroy slave unit

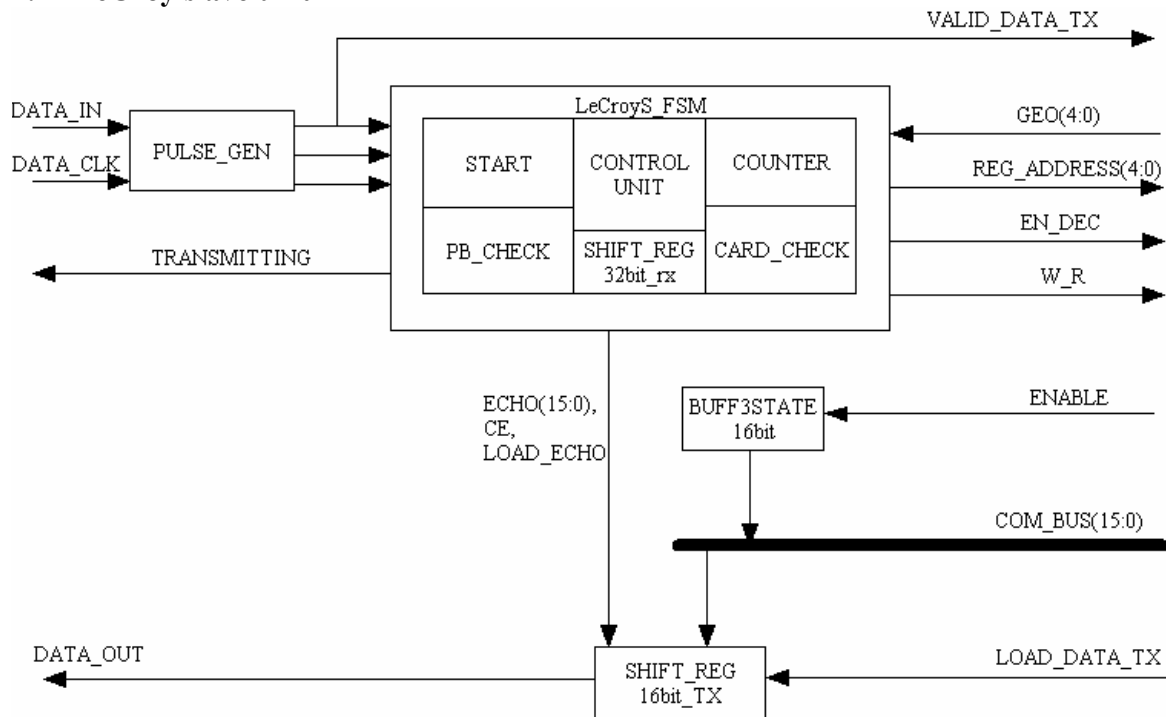


Figure 2

Top-level of the LeCroy slave unit

The LeCroy slave unit is composed by several sub-units, anyone doing its own function.

- *PULSE_GEN*: this module generates a pulse at the rising edge ($VALID_DATA_RX$, Fig. 3) and at the falling edge ($VALID_DATA_TX$) of $DATA_CLK$. These signals are then used as enables by the other modules, for the receiving and for the transmitting cycle respectively. Also the $DATA_IN$ signal is synchronized with $MASTER_CLK$ by using two D-type positive edge-triggered Flip-Flops. For the pulse generating, 3 flip-flops are used, to avoid metastability effects.

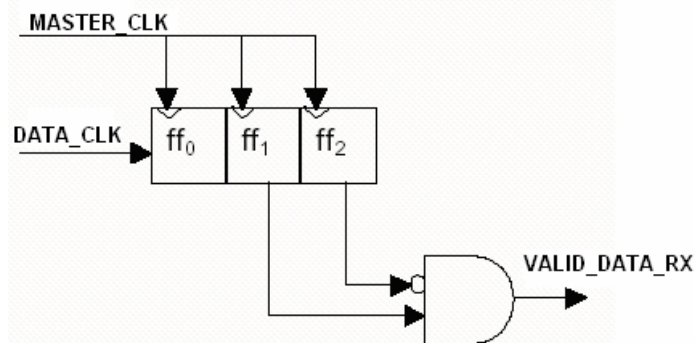


Figure 3

- *shiftreg_16bit_TX*: this is the 16-bit shift register used for transmitting data on the LeCroy interface. It has 2 different signal to load the data: $LOAD_ECHO$ allows the load of the 16

echo bits, while LOAD_DATA allows the load of the 16 data bits. The CE and VALID_DATA_TX signals allow the shift operations.

- *LeCroyS_FSM*: this is a finite state machine, composed by 4 states, describing the LeCroy protocol cycle. The initial state, “state0”, is the one set by the RESET_N active low signal. If a sequence of ‘0’ and ‘1’ is detected, then the cycle begins and the next state is “state_listening”. In this state, bits from the master are written in a shift register (shift_reg_32bit_rx), the parity bit is checked and a 6 bit counter is incremented. When the last bit is in the DATA_IN signal, then the CHIP_ADDRESS (GEO) is checked, together with the parity bit, and if the check is true, then the LOAD_ECHO and enable (CE) signals of the shiftreg_16bit_TX are asserted. The next state is state_reply. Otherwise, if the parity is wrong or the address is different from GEO signal, then next state is state_waiting. In the state_waiting, the counter is incremented but nothing is done; state0 is reached at the end of the 64-bit LeCroy cycle, to allow a new LeCroy cycle. In the state_reply, the LOAD_ECHO signal is negated, while the enable allows the shiftreg_16bit_TX to transmit the bits. One cycle before finishing the echo, the EN_DEC signal is asserted, to enable the decoder; this allows the reading of the 16-bit data to load (LOAD_DATA) on the shiftreg_16bit_TX. When finishing the 64-bit cycle, the state0 is reached, to allow a new LeCroy cycle. There is also a process that generates the TRANSMITTING (SCCE) signal for the LeCroy interface: VALID_DATA_TX signal allows this signal to be asserted.
- *buff3state_16bit*: this is a 16-bit buffer tri state; it is enabled from the arbiter to put its inputs (received data from LeCroy interface) on the “COM_BUS”.

1.2 Data handling architecture

The block TOP_S9011AT consists in a common bus architecture as shown in Fig. 4, with a decoder, the input buffers tri state and the write registers.

- *decoder_S9011AT*: it manages the enables of the registers (for writing operations) and the enables of the buffer tri state (for reading operations). There are 2 types of “reading enable” signals: one for the common inputs of the 2 LeCroy units and the other one for the auto clear registers, that must use different signals between the 2 LeCroy units. As a matter of fact, the auto clear registers are duplicated, to allow the auto clear function (see figure 1.4). The auto clear function is implemented with a D-type flip-flop: the registered input (enable) is used to clear the registers one cycle of clock after the reading operation.
- *SEL register*: it is auto clear, so it is cleared when it is read; it can also be cleared if it is written ‘1’ on the bit 0 of the register 0000 (CLEAR_SEL_1 and CLEAR_SEL_2).
- *glitch_det*: it is formed by 2 D-type flip-flops, one detecting the falling edge, and the other one detecting the rising edge of the input; the output is the OR of the 2 flip-flops outputs.
- *DST_L_trips and DST_H_trips registers*: they are composed by 9 glitch detectors (glitch_det).

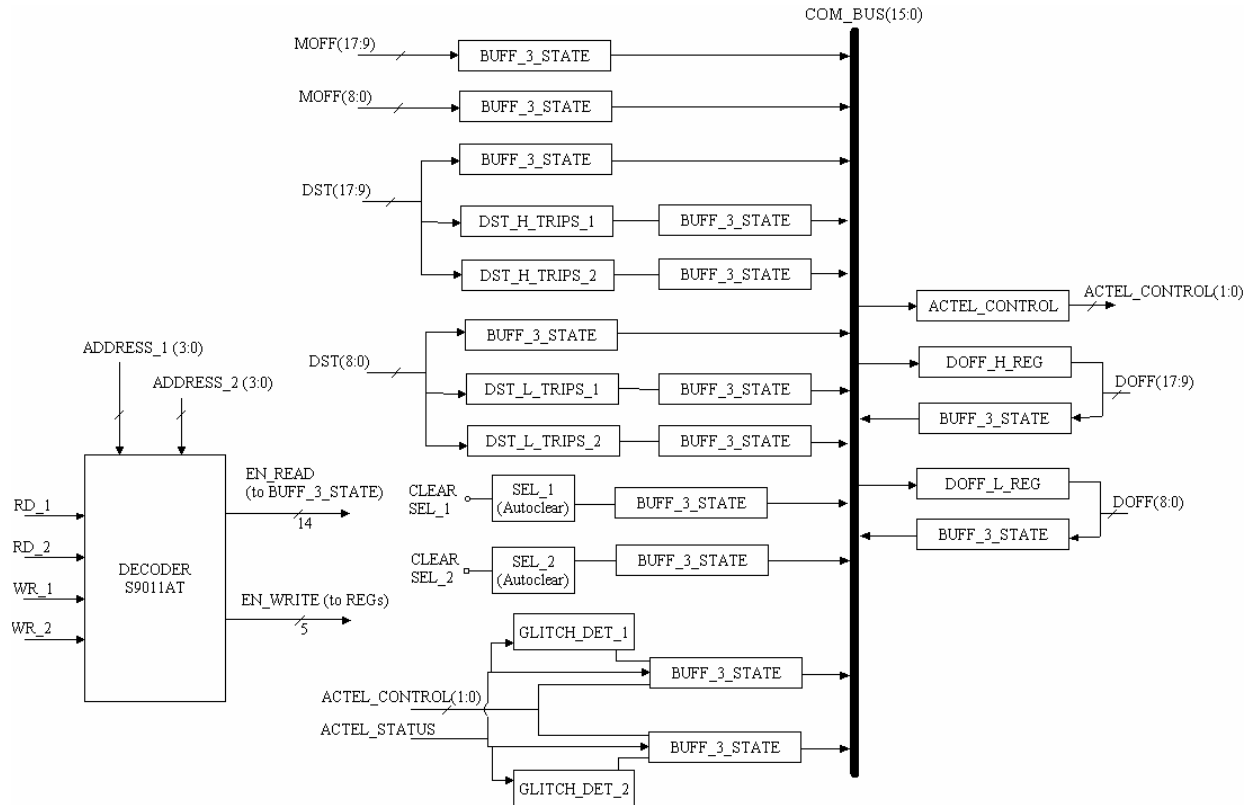


Figure 4

Common bus architecture of the S9011AT

- *DOFF_H reg and DOFF_L reg*: they can be written, and the last values can be read back through the buffer tri state.
- *ACTEL_CONTROL*: it is a special register with the default value 0002h.

2 Description of the VHDL code for the TPSFE board

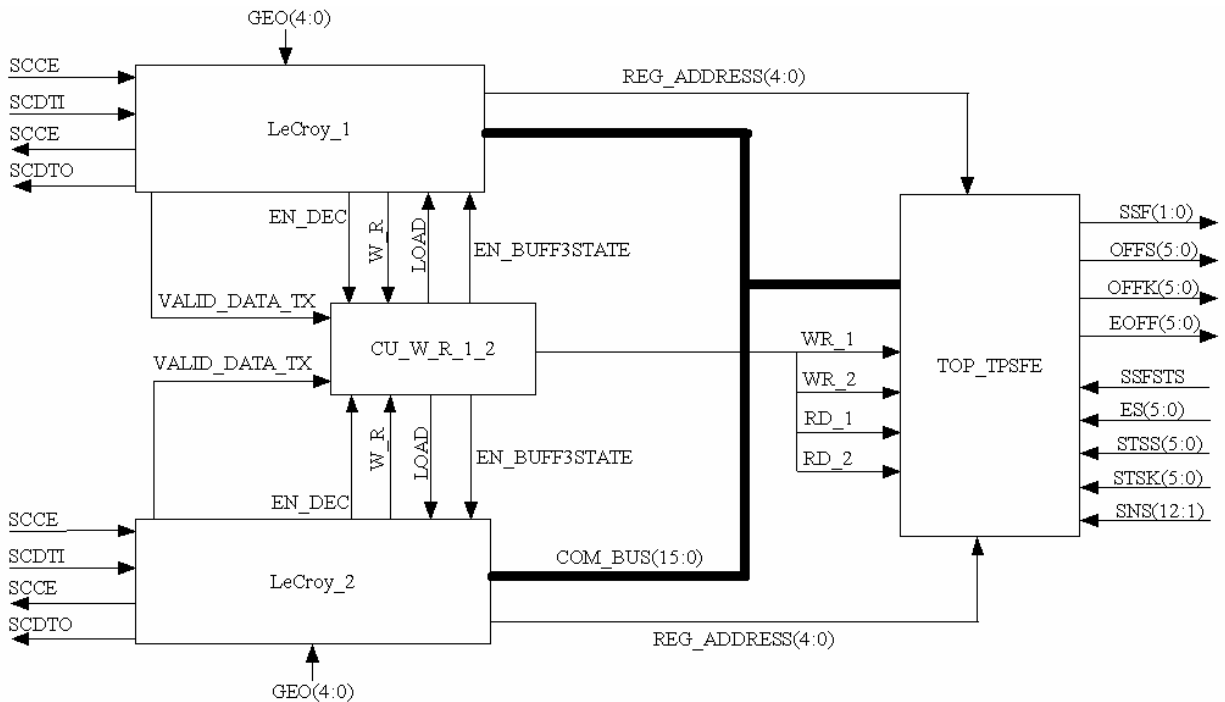


Figure 5

Top-level of the TPSFE's FPGA

2.1 Data handling architecture

The block TOP_TPSFE, shown in Fig. 6, consists in a common bus architecture, with a decoder, the input buffers tri state, the write registers and the TOP_COUNTERS block.

- decoder_TPSFE: it manages the enables of the registers (for writing operations) and the enables of the buffer tri state (for reading operations). There are 2 types of “reading enable” signals: one for the common inputs of the 2 LeCroy units and the other one for the auto clear registers, that must use different signals between the 2 LeCroy units. As a matter of fact, the auto clear registers are duplicated, to allow the auto clear function (see figure 1.4). The auto clear function is implemented with a D-type flip-flop: the registered input (enable) is used to clear the registers one cycle of clock after the reading operation.
- SEL register: it is auto clear, so it is cleared when it is read; it can also be cleared if it is written ‘1’ on the bit 0 of the register 0000 (CLEAR_SEL_1 and CLEAR_SEL_2).

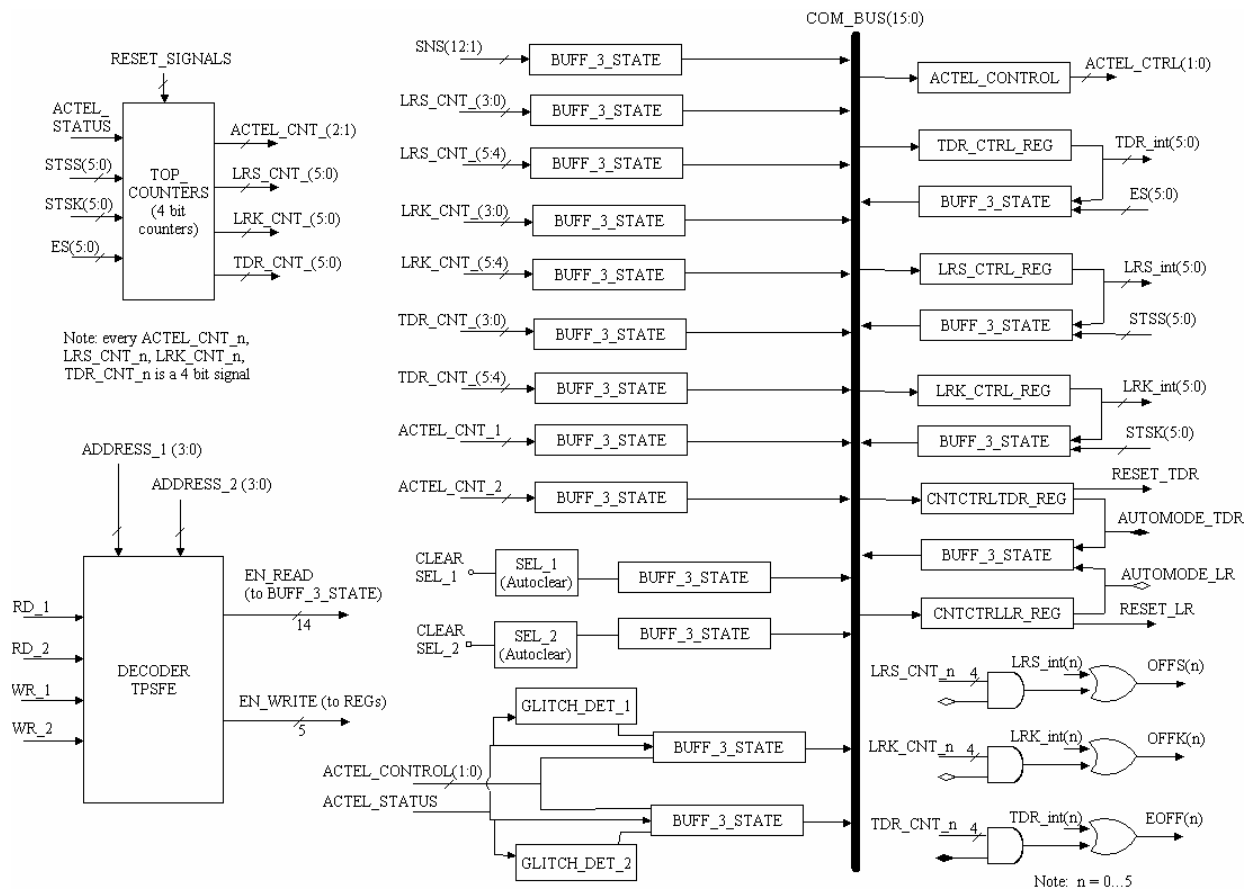


Figure 6

Common bus architecture of the TPSFE

- glitch_det: it is formed by 2 D-type flip-flops, one detecting the falling edge, and the other one detecting the rising edge of the input; the output is the OR of the 2 flip-flops outputs.
- ACTEL_CONTROL: it is a special register with the default value 0002h.
- TOP_COUNTERS: it is a set of counters, as shown in the Fig. 7.
- PRESCALER: it generates a “SCALED_CLK” signal, used for sampling the inputs of the PULSE_CNT blocks. The “SCALED_CLK” samples the input signals at the rising edge, every 32µs.
- PULSE_CNT: it detects every rising edge of the input and increment the 4-bit counter. When the counter reaches “1111”, it stays in that state. There is a clear signal to reset the counters. The ACTEL_STATUS counters are autoclear, while the others get the CLR signal respectively from registers “0111” and “1000”.

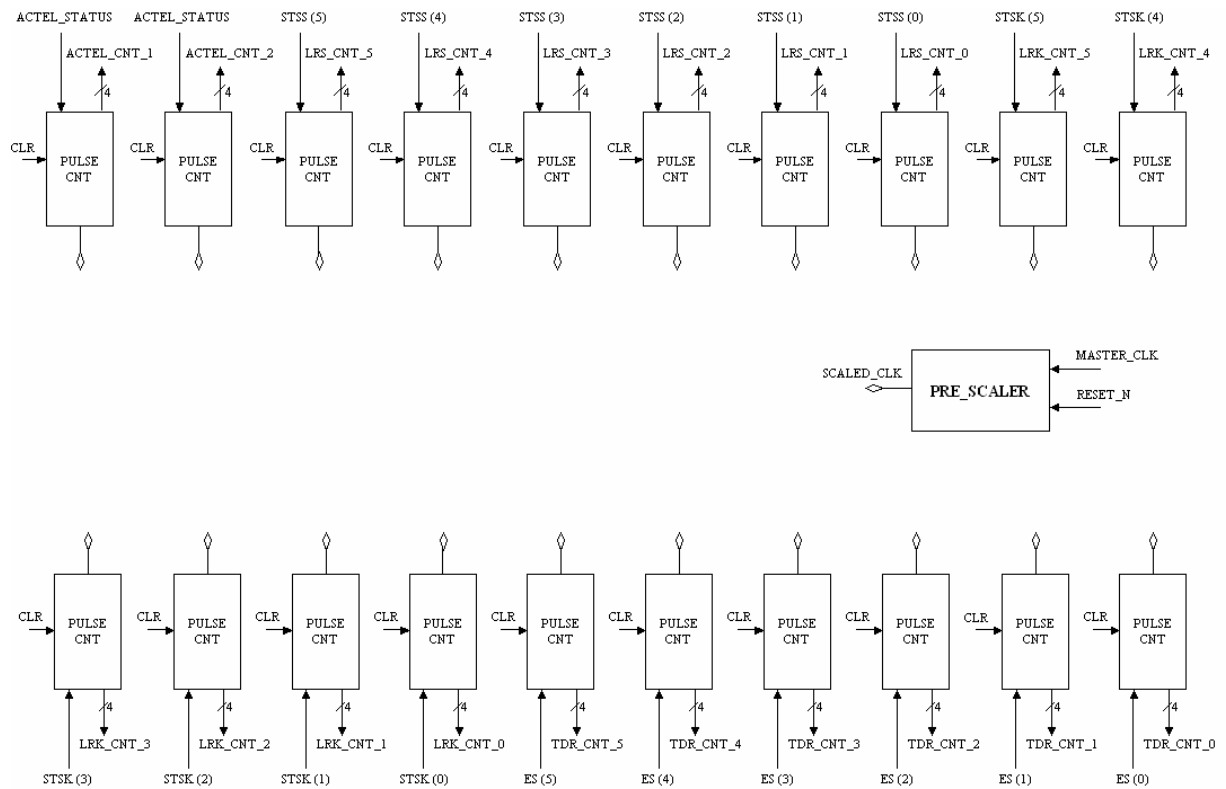


Figure 7
TOP_COUNTERS architecture of the TPSFE