# AMS-TIM Meeting

*Cern, January 15, 2004*

# Status Report on AMS Tracker Thermal Control System (TTCS)

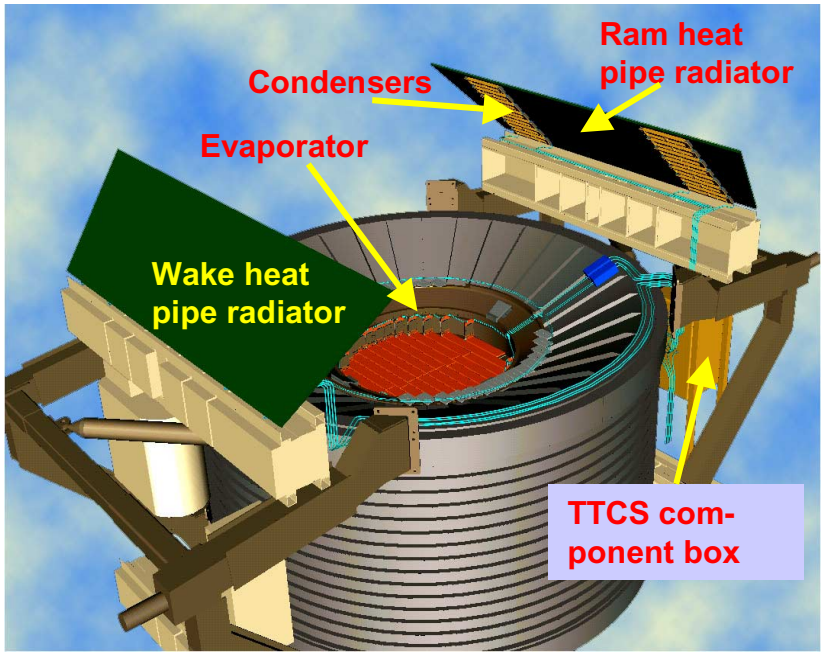
## TTCS Electronics

Johannes van Es (NLR),

Carlo Rens (NLR), Jacob Jaarsma (NLR)

## Contents

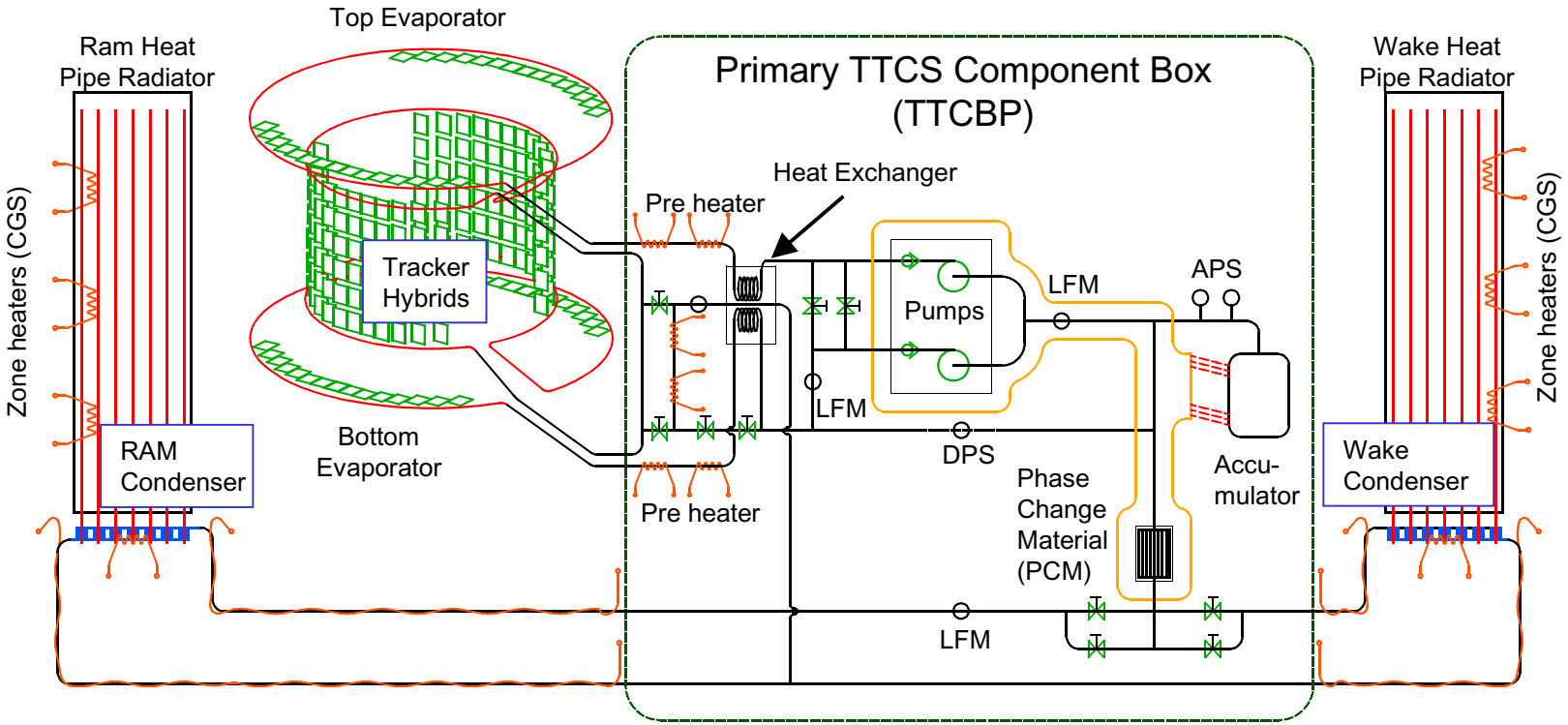
- TTCS Overview
- TTCS Electronics overview
- TTCS Control Lay-out
- TTCS Block diagram
- Sensor & Actuator board
- TTCE Block Diagram
- Component selection
- Cabling
- Electronics Status



## TTCS Overview

- Two redundant carbon dioxide two-phase loops (both capable to fulfil the AMS-Tracker req's)
  - Primary loop (with valve controls, experiment by-pass, LFM's)
  - Secundary loop (current status, no valves, no experiment by-pass, no LFM's)

# Primary TTCS (TTCSP)




2-Way Valve (VLV)

Centrifugal pump (PMP) with integrated check valve

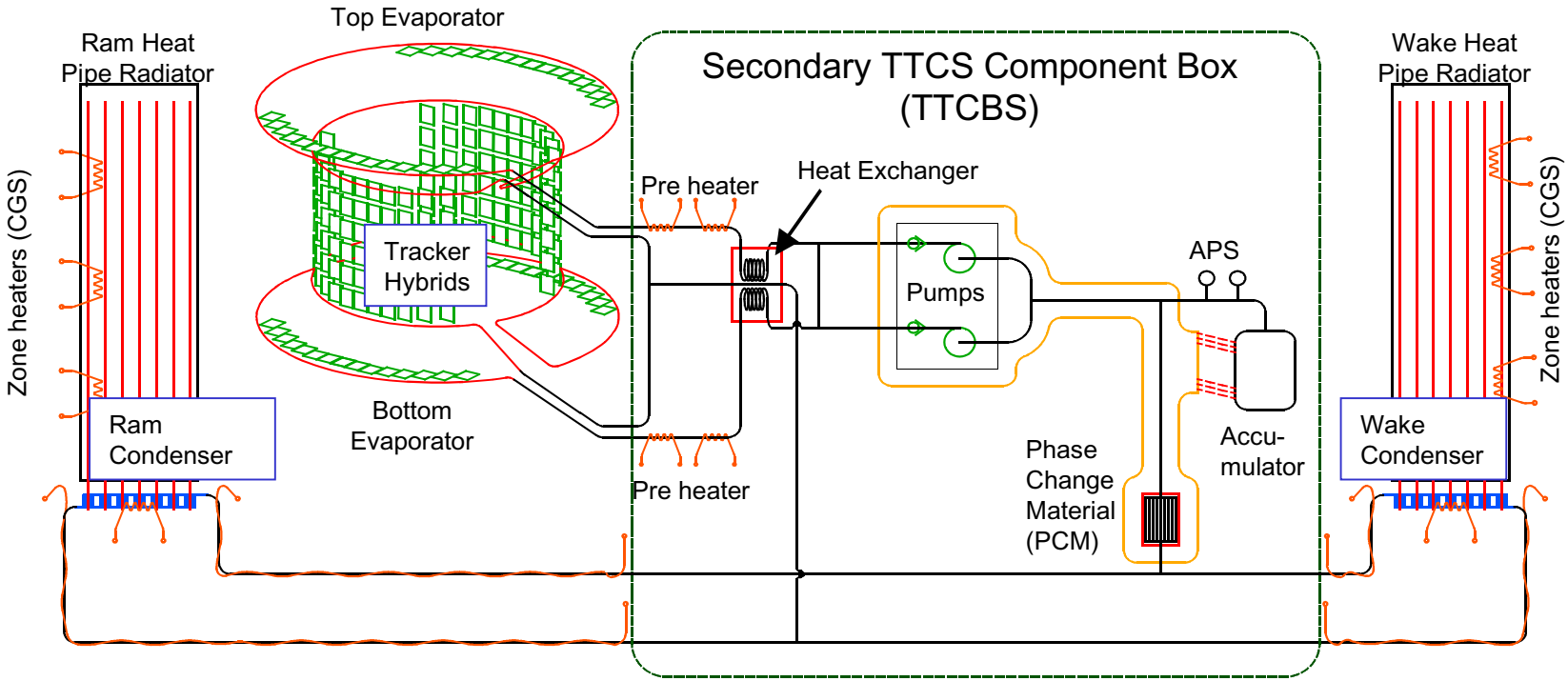
Electrical Heater (HTR)

Sensors:
LFM = Liquid Flow Meter,
DPS = Differential Pressure Sensor
APS = Absolute Pressure Sensor
VQS = Vapor Quality Sensor

Components inside this profile are thermally mounted to the TTCB structure

Thermo Electric Cooler (TEC)

# Secondary TTCS (TTCSS)




2-Way Valve (VLV)

Centrifugal pump (PMP) with integrated check valve

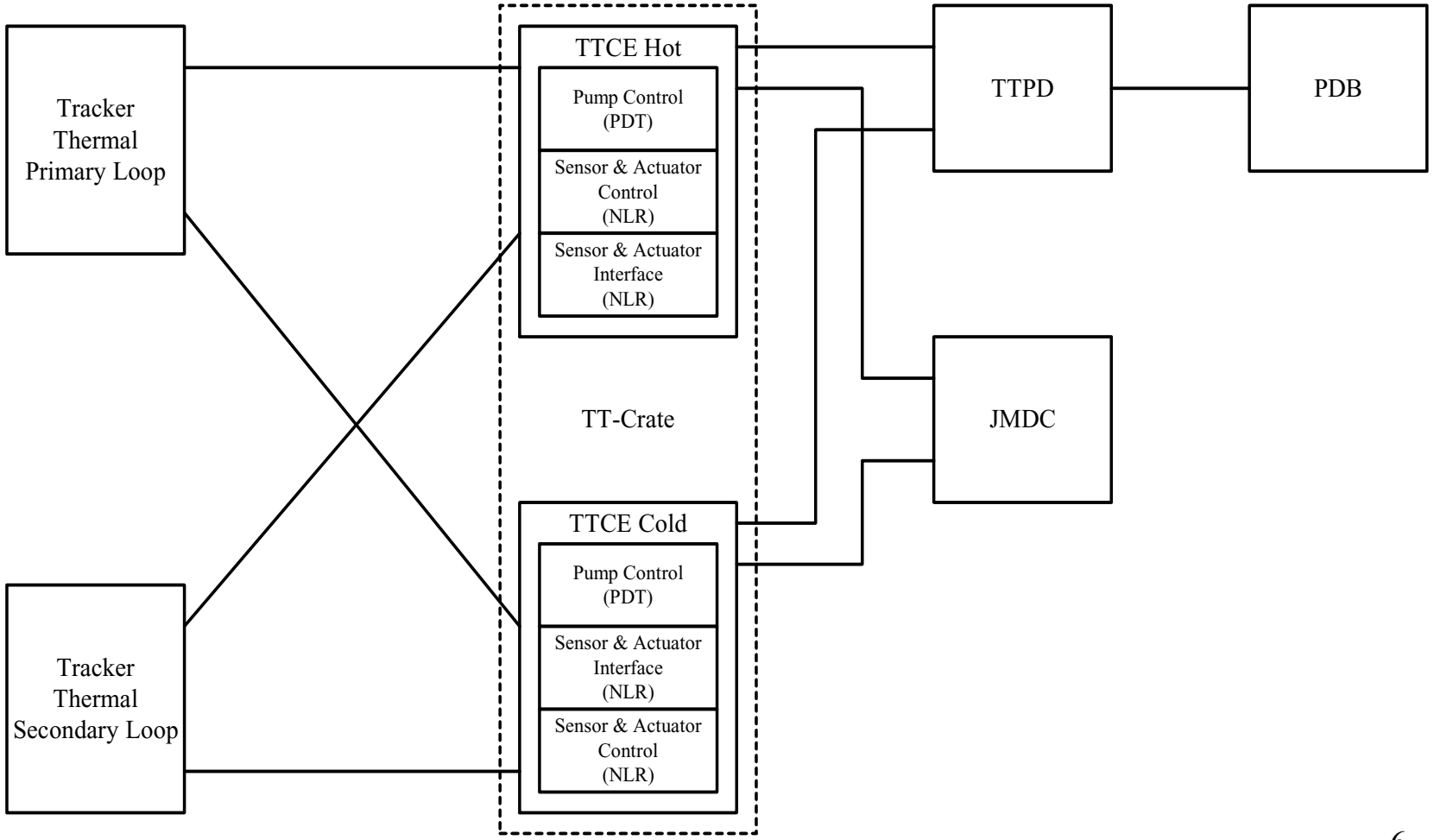
Electrical Heater (HTR)

Sensors:
LFM = Liquid Flow Meter,
DPS = Differential Pressure Sensor
APS = Absolute Pressure Sensor
VQS = Vapor Quality Sensor

Components inside this profile are thermally mounted to the TTCB structure

Thermo Electric Cooler (TEC)

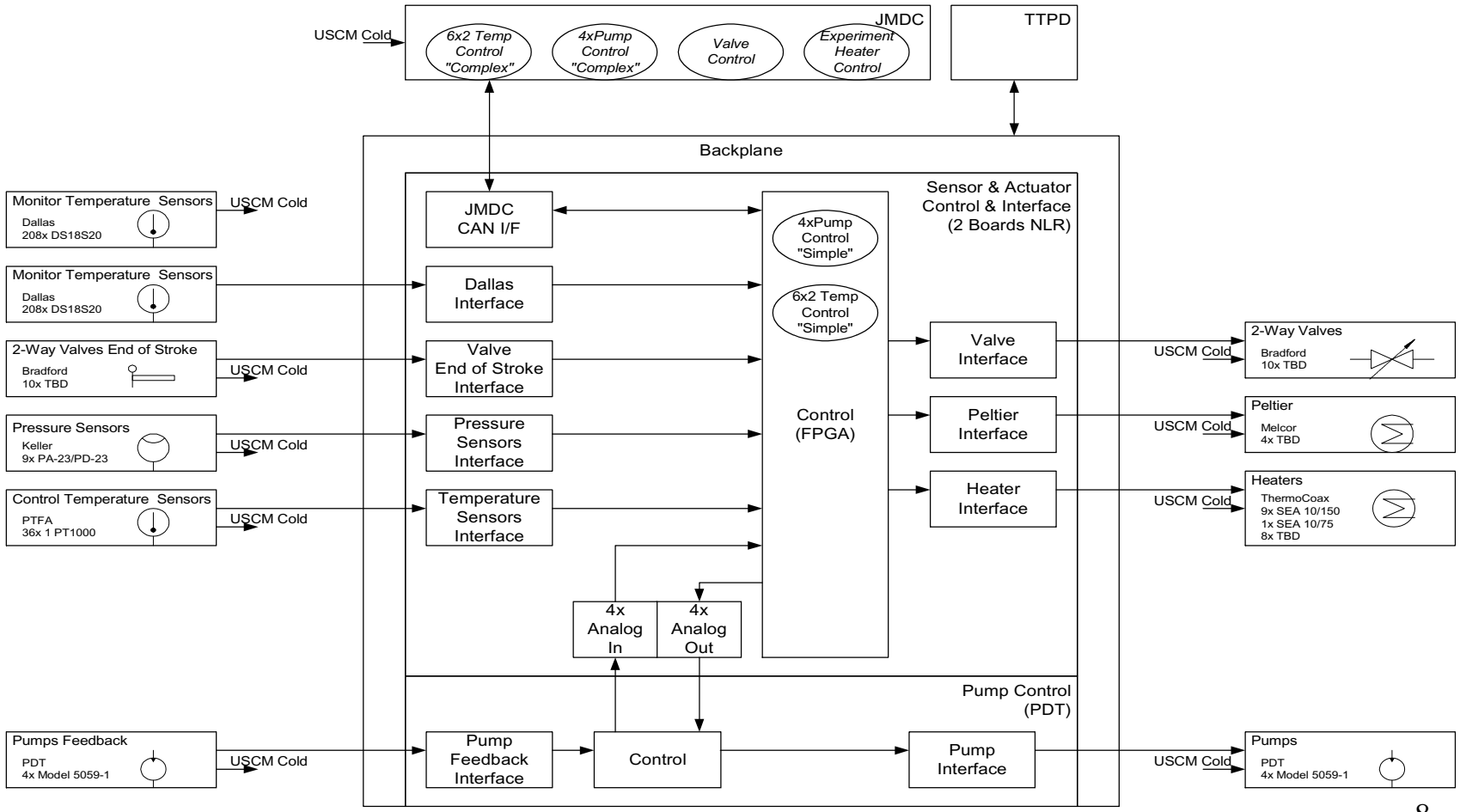
# Technical status: Electronics (Overview)



## TTCS control layout

- TTCE full redundant for primary and secondary loop
- Pure cold redundancy between loops
- High level control loops on mission computer
  - "complex" temperature/pre-heaters control
  - experiment heaters control
  - valve control
- Low level "simple" control available for peltiers and pre-heaters on sensor & actuator board

# Technical status: Electronics (TTCE Block diagram)



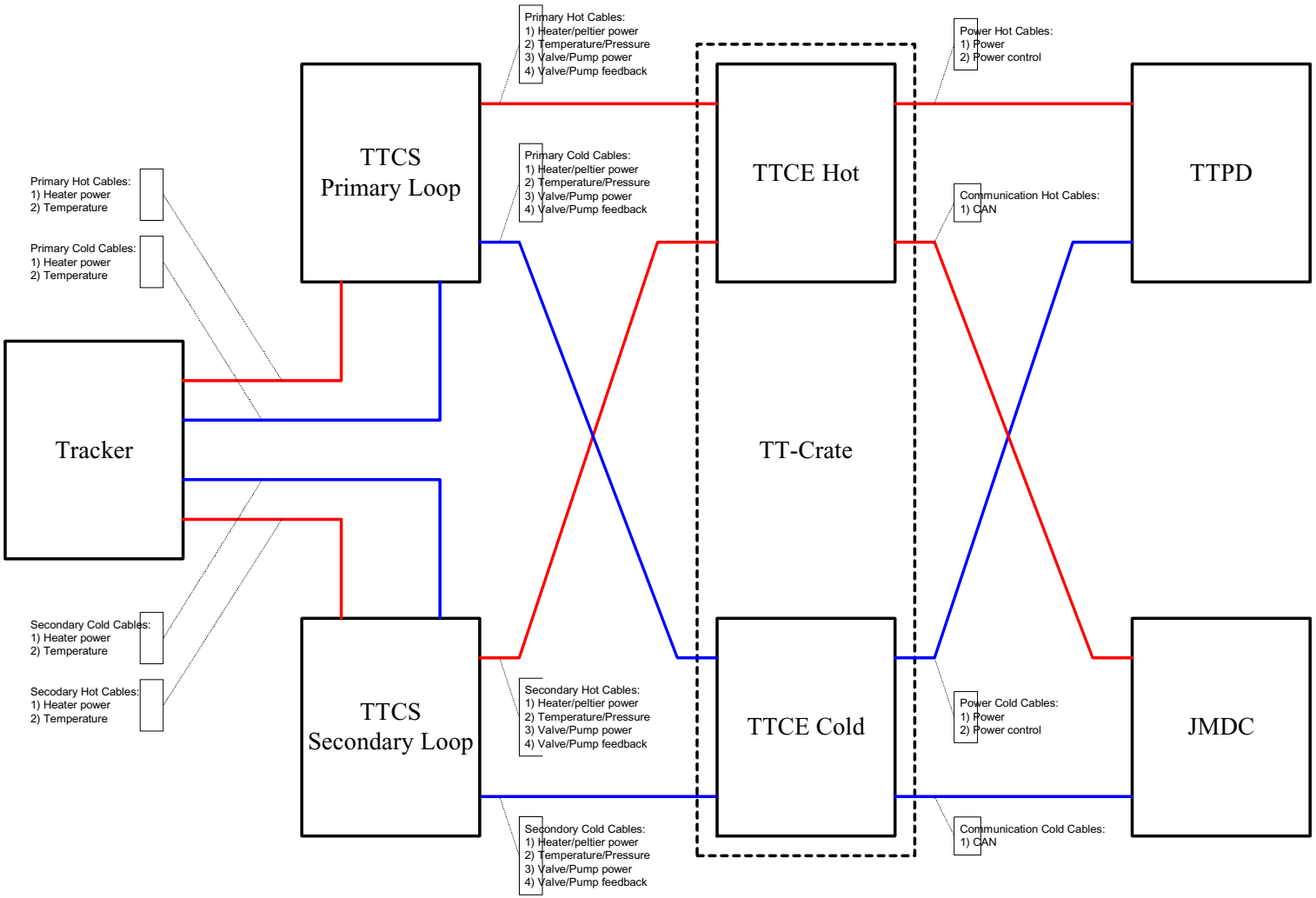
## Sensor & actuator board

- Temperature & pressure sensor interface
  - Proven design from earlier NLR space project
- Valve
  - On/Off (TBC)
- Experiment heater interface
  - 28V on/off control
- Peltier / pre heater interface
  - Thermoelectric Cooler Controller (PWM control)
- USCM interface
  - 16x digital I/O + 8x address
- Local Control
  - FPGA

## Component selection

- Selection Criteria
  - From PPL
  - SEE free
  - Add latch-up protection
- Thermoelectric Cooler Controller Candidates
  - ADN8830, LTC1923, MAX1978
- Preferred FPGA
  - Xilinx XQR4000XL with XQ1701L (PROM)

# Electronics (Cabling)



# Technical status: Electronics

## Power budget update

| Item | Type | Voltage [V] | Power Single [W] | Primary loop Units Nom [ ] | Primary loop Units Redun [ ] | Secondary loop Units Nom [ ] | Secondary loop Units Redun [ ] | Secondary loop Units Exp. | Power Primary Nom Total (1) [W] 156.08 | Power Primary Avg. Total (4) [W] 82.08 | Power Primary Remarks No design values! | Overall AWG Total (5) [W] 231.08 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Pump | PDT 5059 | 28 | 10 | 2 | | 2 | | 1 | 20.00 | 10 | 1 pump 50% active | 20 |
| Valve | | 28 | 7 | 1 | | | | 1 | 7.00 | 7 | Limited in time but 10 | 7 |
| Pre heater | SEA 10/150 | 28 | 25 | 2 | 2 | 2 | 2 | | 50.00 | 30 | 60% active TBC | |
| Exp heater | SEA 10/150 | 28 | 50 | | | | | 1 | | 0 | % active | 50.00 |
| Exp heater | SEA 10/75 | 28 | 75 | | | | | 1 | | 0 | % active | 75.00 |
| Peltier | | 28 | 20 | 1 | 1 | 1 | 1 | 1 | 20.00 | 16 | 80% active | 20.00 |
| Accu. heater | Minco Foil | | 40 | 1 | | 1 | | 1 | 40.00 | 0 | % active | 40.00 |
| APS | | 28 | 0.2 | 2 | | 2 | | 2 | 0.40 | 0.40 | | 0.40 |
| DPS | | 28 | 0.2 | 1 | | 1 | | 1 | 0.20 | 0.20 | | 0.20 |
| LFM | | 28 | 0.2 | 4 | | | | 4 | 0.80 | 0.80 | | 0.80 |
| DTS | DS1820 | 5 | 0.003 | 208 | | 208 | | 208 | 0.62 | 0.62 | | 0.62 |
| MTS | PTFA Pt-1000 | 5 | 0.003 | 18 | | 18 | | 18 | 0.05 | 0.05 | | 0.05 |
| | | | | | | | | | | | | |
| TT-Crate | | | | | | | | | | | | |
| | PDT | | 5 | 1 | 1 | | | 1 | 5.00 | 5.00 | | 5.00 |
| | S&A | | 10 | 1 | 1 | | | 1 | 10.00 | 10.00 | | 10.00 |
| TTPD | | 28 | 2 | 1 | 1 | | | 1 | 2.00 | 2.00 | | 2.00 |

## *Technical status: Electronics (Design Issues)*

TT-Crate without USCM boards is possible:

- S&A board with CAN I/F for JMDC communication
- Dallas interface & readout on S&A board (initialisation via JMDC)

Advantages

- 3 boards (2x S&A & 1x PDT)  (was 4 with USCM)
- Hot/cold electronics can be separated if needed
- More simple backplane
- Improvement of  testability S&A boards
  (EGSE is power & CAN interface)

## *Technical status: Electronics*

**Electrical in progress**

- **S&A board layout**
- **Detailed design FGPA (VHDL)**

**Open items:**

- **Higher level CAN protocol definition (for option without USCM)**
- **Requirements/information on JMDC algorithm development**
- **Detailed Information on 3V & 5V DC/DC boards**

**To Do Electrical:**

- **Implementatiom simple & complex algorithms/scenarios**
- **Design 28V & ±15V DC/DC boards**
- **Design backplane TT-crate & TTPD**