

AMS-02 Scintillator Electronics Status

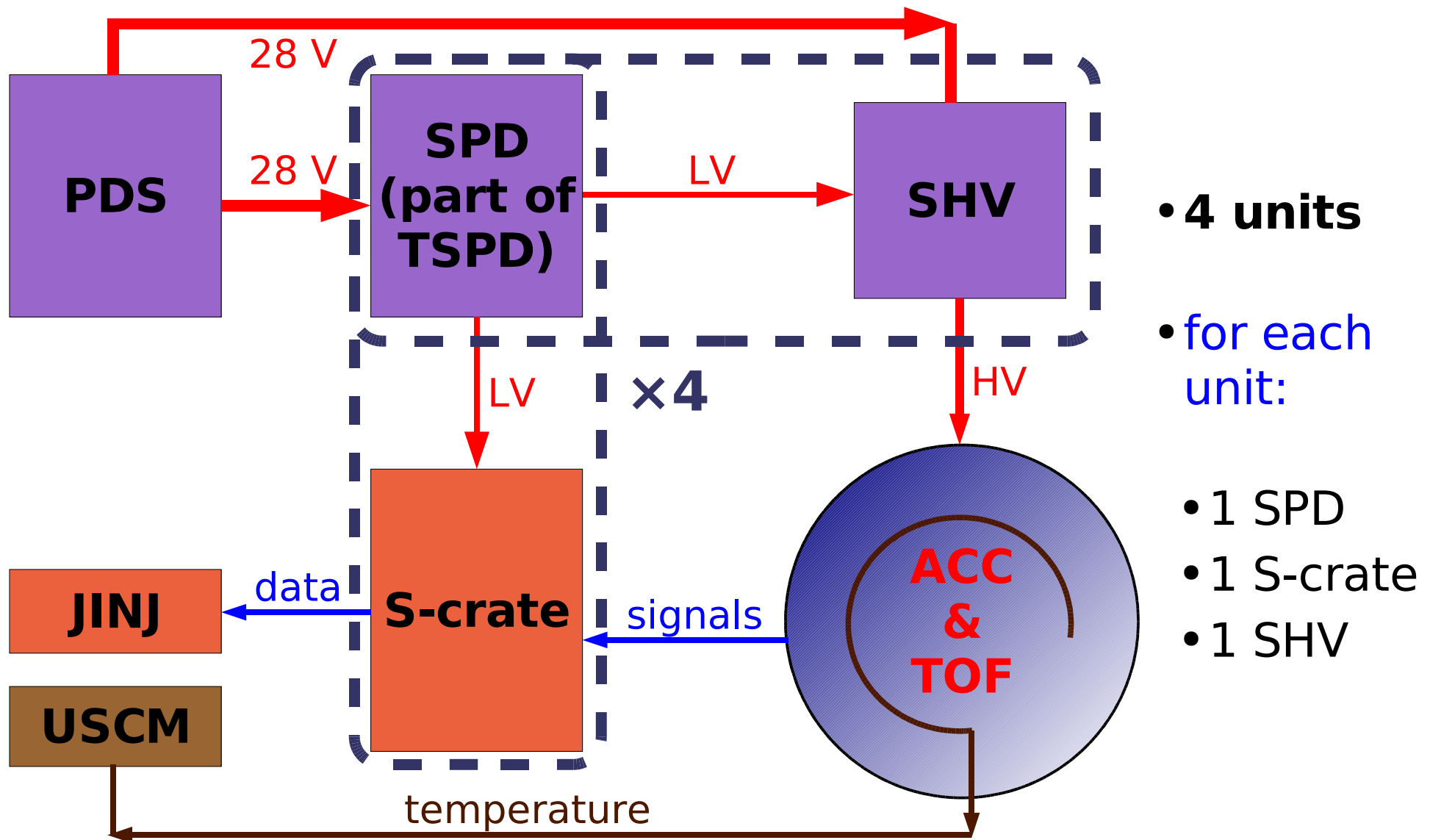


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AMS TIM @ CERN, 30 Jan – 3 Feb 2006

Scintillator electronics system



Scintillator electronics

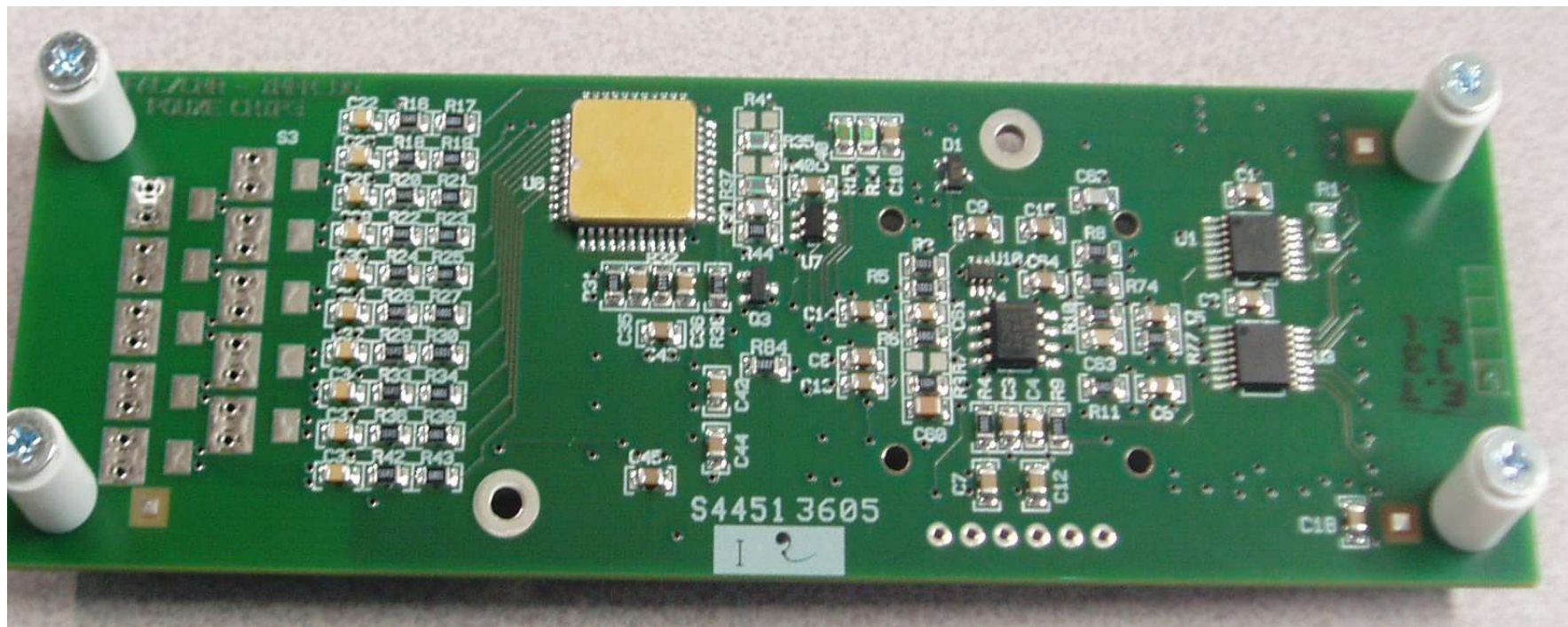
- *Power supplies for ACC and TOF:*
 - Inside SPD: **S9074** (3.4 V, 5.6 V), **S9052** (± 5.6 V)
 - **SHV**: high voltage
- *Front-end electronics:*
 - **SDR2**: data collection and reduction
 - **SFEC**: charge (*inside TOF*; dynodes)
 - **SFET2**: charge and time (TOF anodes)
 - **SFEA2**: charge (ACC, TOF) and time (TOF)
 - **SPT2**: pre-trigger unit
- *Each of the 4 **S-crates** contain:*
 - 1 SDR2
 - 4 SFET2
 - 1 SPT2 (hosting connectors for 2 SFECs)
 - 1 SFEA2

Power supplies

- **SHV:**
 - QM2 and FS in production: delivery on feb – apr 2006
 - FM production (4 SHVs) in 2007
- **S9074, S9052:**
 - QM2 available since several months for testing
 - FM in production (with no coating until final OK)

SFEC

- QM thermal test between -40 C and +75 C (operative):
 - Less than 5% gain variation in [-20 C, +55 C]
 - Dynamic range \approx 4 – 800 MIPs
- FM delivered (after thermal stress and thermal cycles at CAEN)
- FM boards to be installed inside LowerTOF next week
- FM test to be carried on inside the TOF



Boards to be produced at CSIST

- QM2 production by CSIST has been financed:
 - 1 backplane (SBP)
 - 1 SDR2
 - 1 SPT2
 - 4 SFET2
 - 1 SFEA2
 - 2 S-crate mechanics
- QM2 tests scheduled this summer in Terni
- In addition:
 - QM1 (FR4) of SBP, SDR2 and SPT2 available in Italy
 - QM1 (FR4) of SFET2 and SFEA2 to be produced
- **Independent setups** will be ready for **CERN** (integration tests), **Bologna** (TOF read-out) and **Aachen** (ACC read-out)

SDR2

- EM/CDP preliminary tested at CERN:
 - AMSwire, slow control interface
- The board failed some test in Italy: the problem was solved on the QM1
- A mismatch in pin assignment was found in front connectors of QM1 and has to be corrected by changing VHDL on the common digital part
- CSIST production started last week
- Interface tests with SFEC, SPT2, SFET2 in progress (FPGA)

SPT2

- Documentation for CSIST ready
- QM1 under test in florence:
 - higher priority given to integration tests (read-out and data acquisition)
 - SFEC interface (data pass-through and power lines) successfully tested
 - link to SDR2 (“TOFwire”) and trigger functions have been developed by Lin: they are **to be tested**
- CSIST waiting for the “Go!” for production

Backplane

- Gerber and documentation for CSIST under review:
 - Some wire is not properly designed and might cause cross-talk effects: the routing is under review
- QM1 assembled for testing and system integration

SFET2, SFEA2

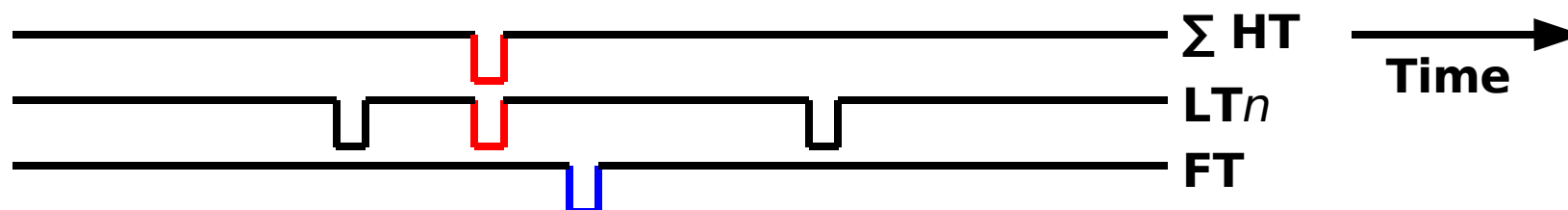
- SFET2 EM under test in Bologna (being stopped for the detector assembly)
- TOFwire link implemented and under test with SDR2
- **Problems discussed at CSIST during last TEM:**
 - LeCroy TDC (PLCC ceramic prototype assembly, AMS-01) are 10 years old
 - The total number is low (no contingency) and production has been discontinued
- **Solution proposed at CSIST and addressed on monday at the electronics splinter meeting:**
 - the new high-performance TDC (HPTDC) developed by CERN for LHC experiments is available
 - 70 pieces have been booked by Florence
 - design and prototyping by CAEN starts now
 - production at CSIST

The new TDC

- **HPTDC:** <http://micdigital.web.cern.ch/micdigital/hptdc.htm>
 - Radiation hard (developed for LHC) ball-grid array
 - 8 channels with 25 ps/bin
- To be connected to a FPGA (Actel) for chip programming and data collection
- Inside S-crates we have 4 slots for TOF front-end cards (SFET2) and 1 slot for ACC front-end (SFEA2), for a total of 18 TOF + 4 ACC channels
 - Using HPTDC we can have a bit more channels on each S-crate: **no channel is lost**
 - No time-expansion needed: simpler design, less components

New configuration

- 4 SFET2 cards per S-crate with HPTDC at 25 ps/bin
- HPTDC inputs:
 - FT, 5 anodes, sum of 5 HTs, sum of 5 SHTs



History can be as long as 64 μ s, but best time window probably goes from $FT - 10 \mu$ s to $FT + 6 \mu$ s (like AMS-01).

HT and SHT measured with same time resolution as LT.

- 1 SFEA2 card per S-crate with HPTDC at 25 ps/bin
- HPTDC inputs:
 - FT, 4 anodes, 3 spare

S-electronics schedule

- Power supplies – goal: FM ready in 2007 (1st quarter)
 - SHV: QM2 + FS delivery in feb–apr; FM in 2007
 - S9052: QM ready; FM in production
 - S9074: QM ready; FM in production
- FE and DAQ electronics – goal: QM2 ready in summer 2006
 - SFEC: FM produced; assembly on LowerTOF this month
 - SDR2: QM1 available in Italy; QM2 in production (CSIST)
 - SPT2: QM1 available; CSIST waiting for the “Go!” (QM2)
 - SBP: QM1 available, needs changes;
 - SFET2: new TDC?
 - SFEA2: new TDC?
 - S-crate mechanics: 2 crates in production at CSIST
- Integration at CERN will start this month