

xDR, JINx Software Status

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MIT

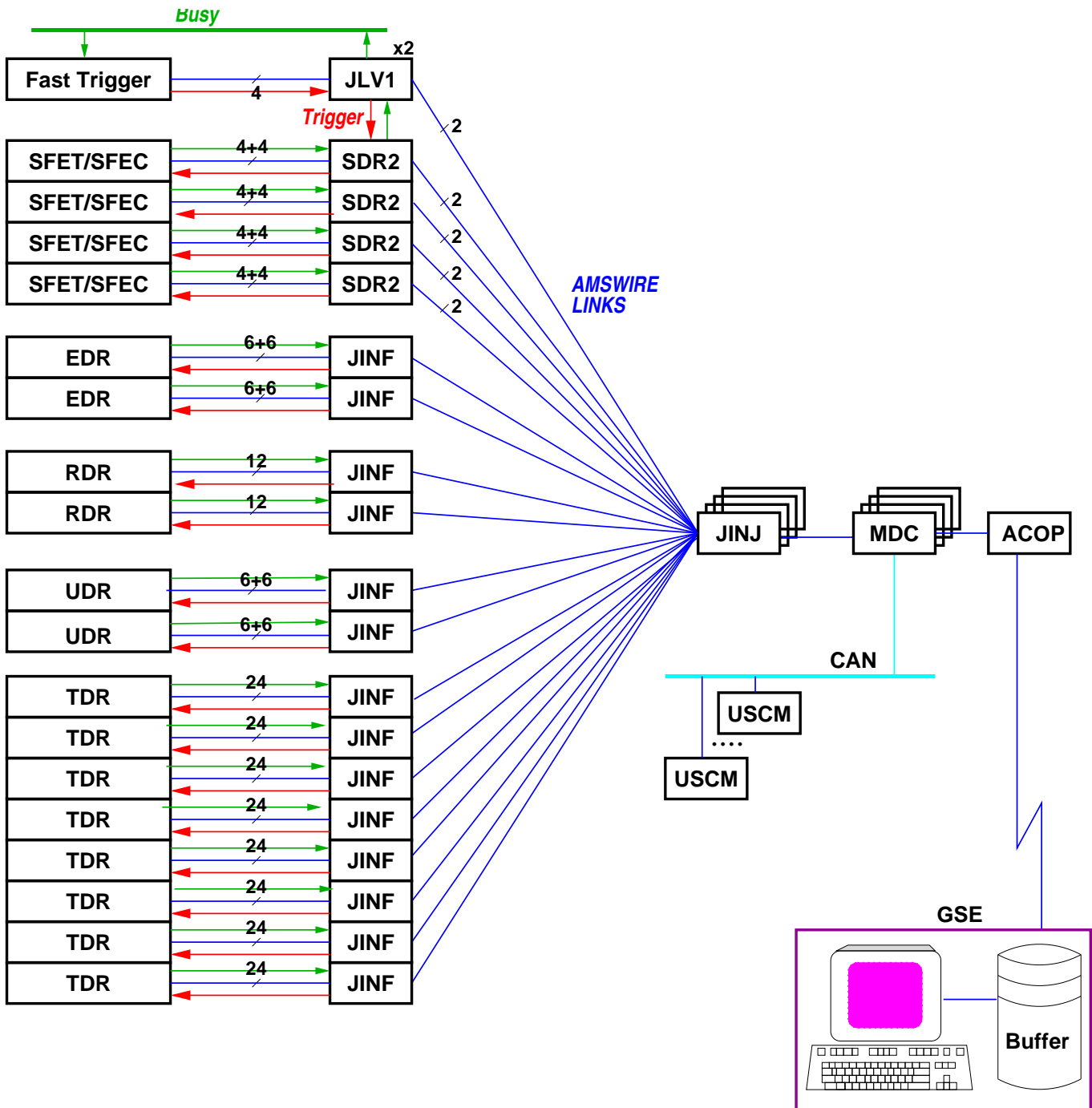
CERN, 22 July 2004

OUTLINE:

- DAQ design considerations
- Software organisation and status
- Tests and performance
- Plans

AMS DAQ system

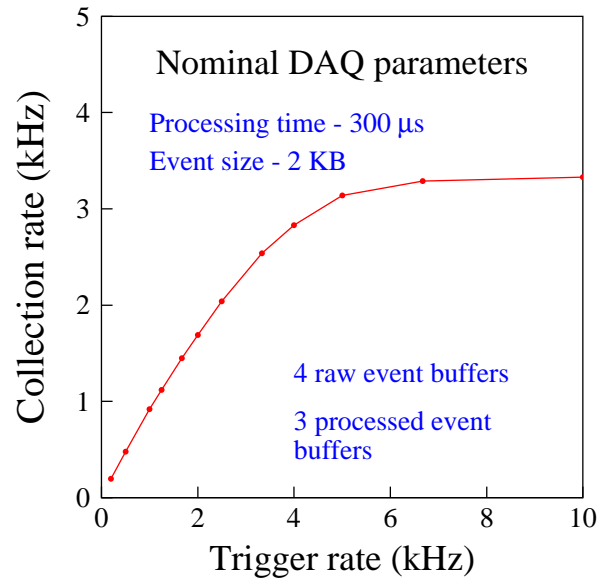
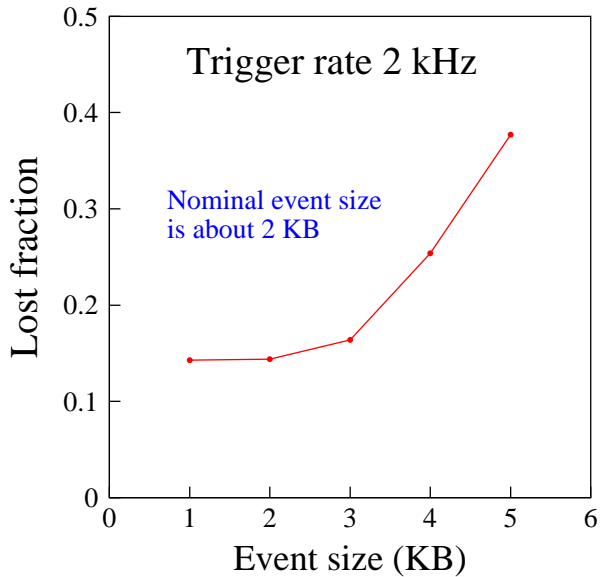
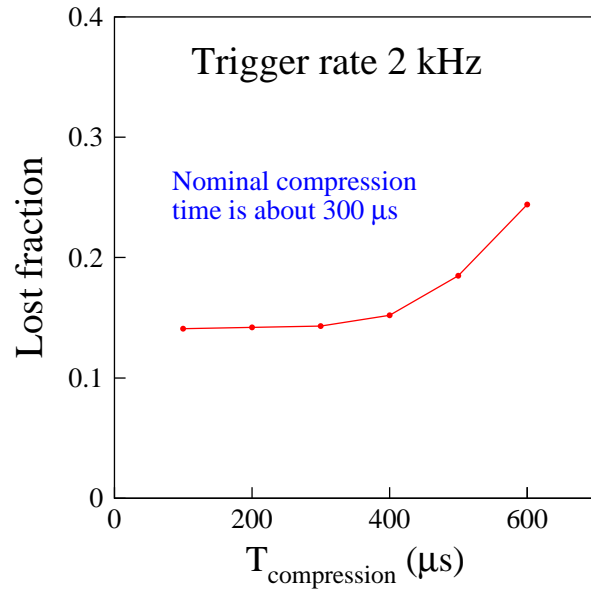
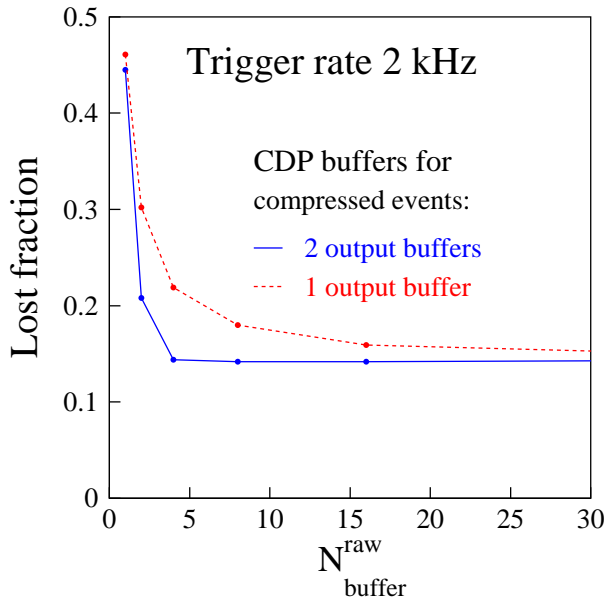
Raw event – 0.6 MByte, processed – 2 KByte.



Event rate: ~ 2000Hz.

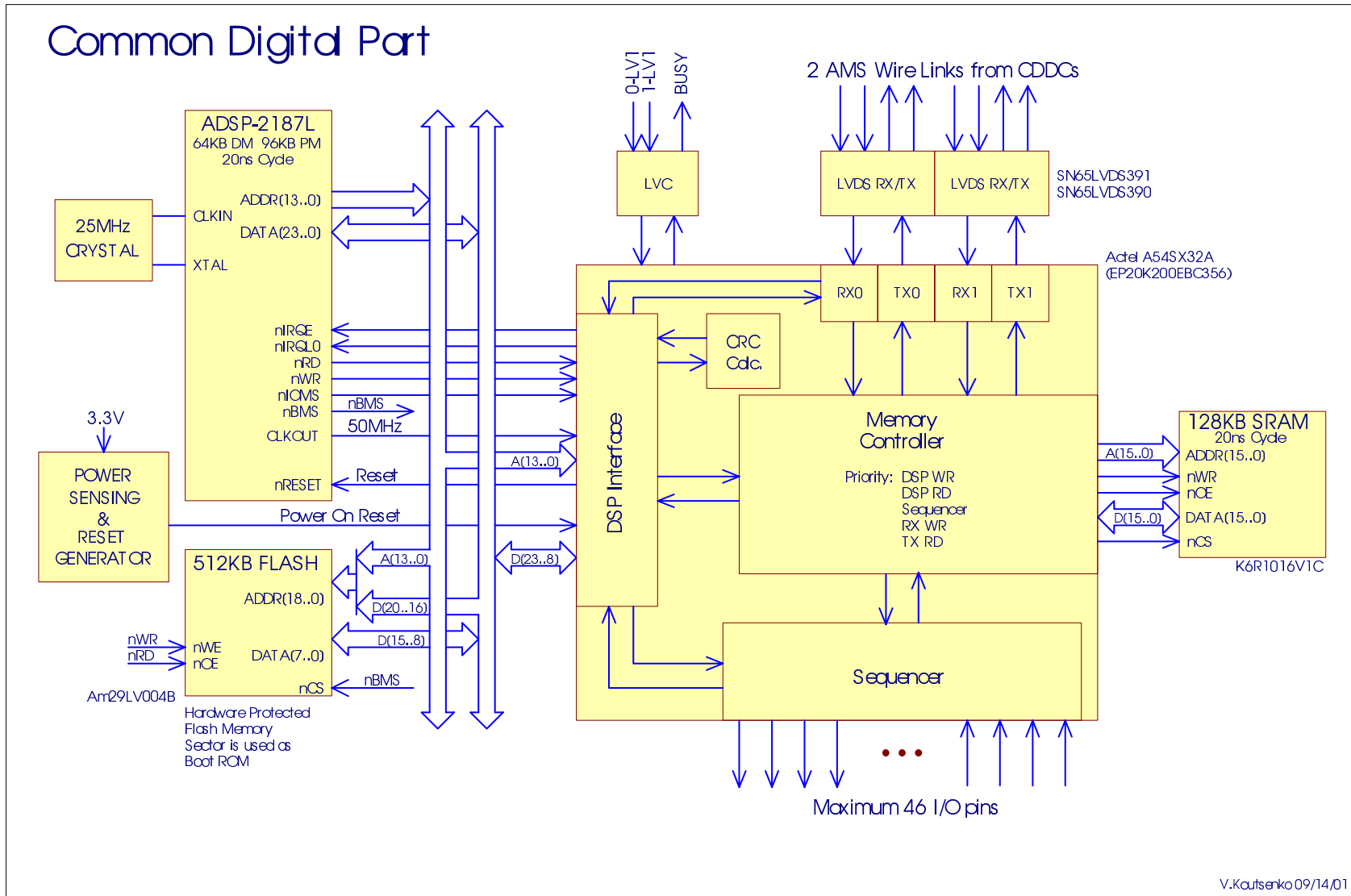
DAQ design studies

MC simulation

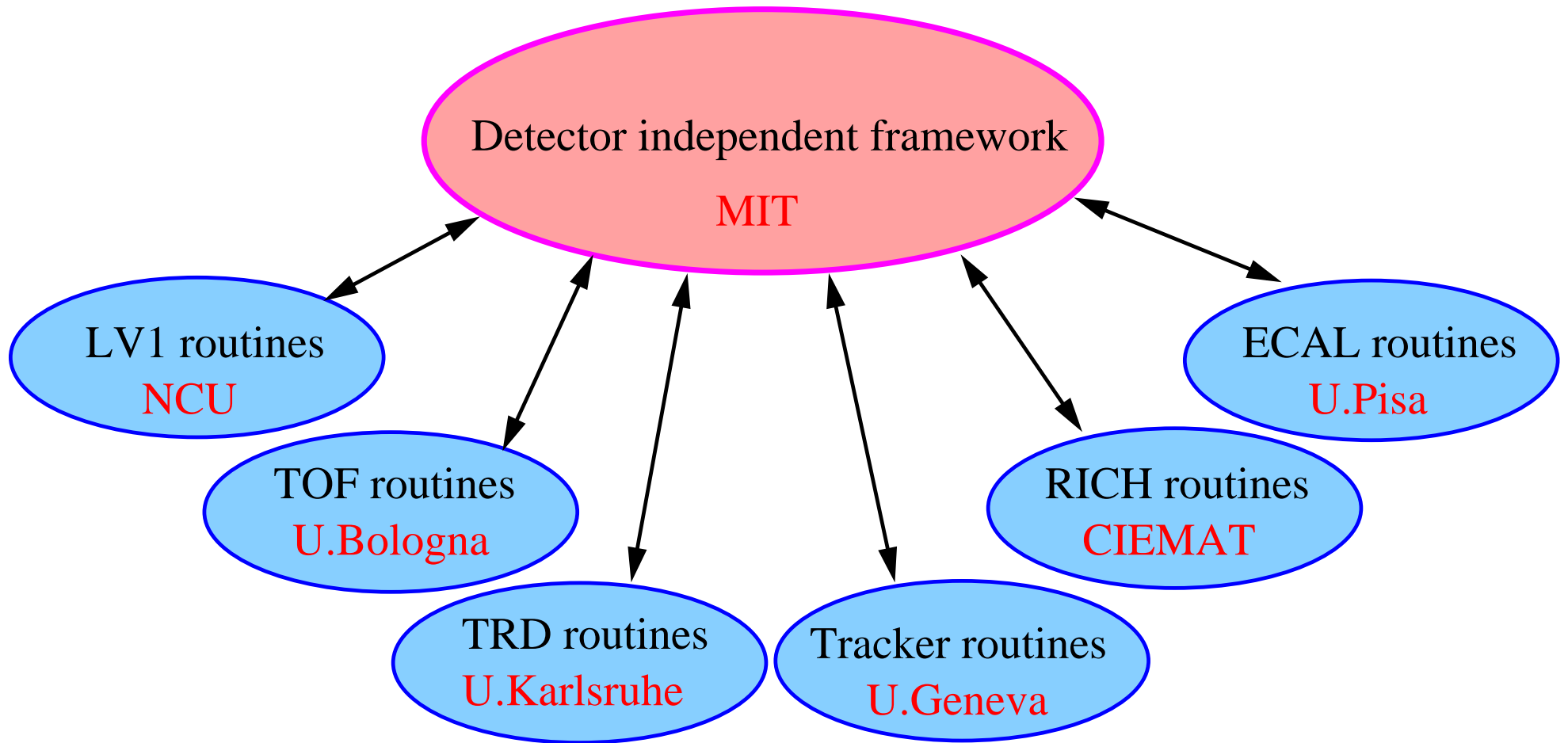


Expected Trigger rate: 200 – 2000 Hz

CDP block diagram



Subdetector software organization



CDP/CDDC software

Ingredients:

Detector independent:

1. Boot procedure;
2. FLASH operations;
3. Data protection;
4. AMSWIRE operations;
5. Event building;
6. In-situ test procedures;

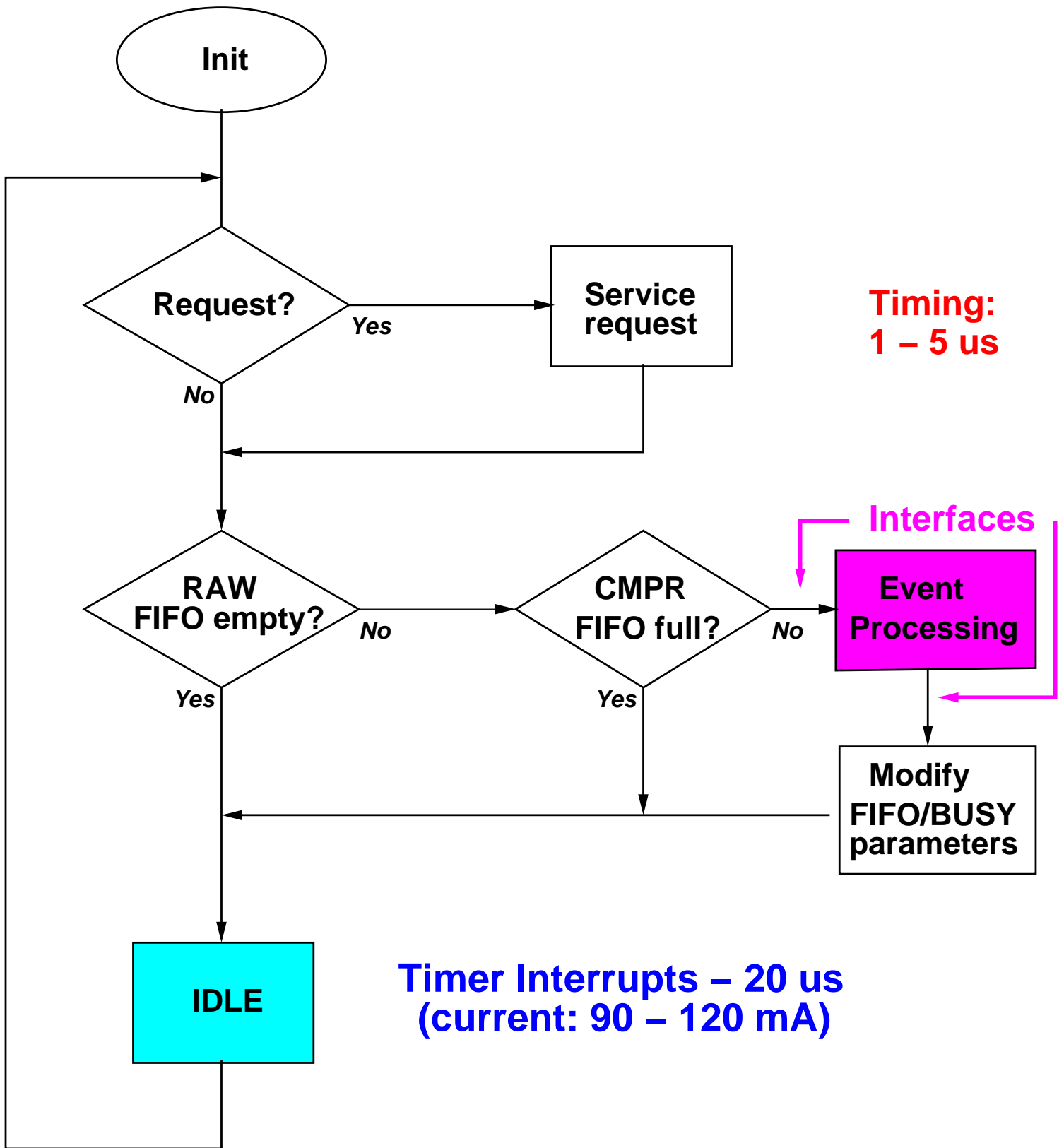
Detector dependent:

7. Data reduction;
8. Calibration procedures;
9. Slow Control and Monitoring.

Subdetectors:

1. Framework (A.Kunin);
2. LV1 Trigger (C.H.Lin);
3. Silicone Tracker (D.Haas);
4. Ring–Imaging Cerenkov Detector (G.Martinez);
5. Transition Radiation Detector (F.Hauler);
6. Electromagnetic Calorimeter (F.Spinella).
7. Time–of–Flight and Anti–Coincidence Counters (F.Cindolo);

Program Flowchart



X-Crate Prototype



U- and J- “crates” in B892



Software status

Tests:

1. Beam tests – TDR, UDR crates;
2. Qualification tests – JT crate;
3. Functional tests – TDR, UDR, JT crates;
4. Functional test – RDR prototypes;
5. EDR, SDR, RDR – HW needed at CERN (now).

Outcome of the tests:

1. Measurements of processing speed, AMSW link throughput;
2. List of “unwanted features” – corrections to SW;
3. Optimisation of processing algorithms (TDR algorithm – $\sim 200\mu s$);

Slow Control in JINF

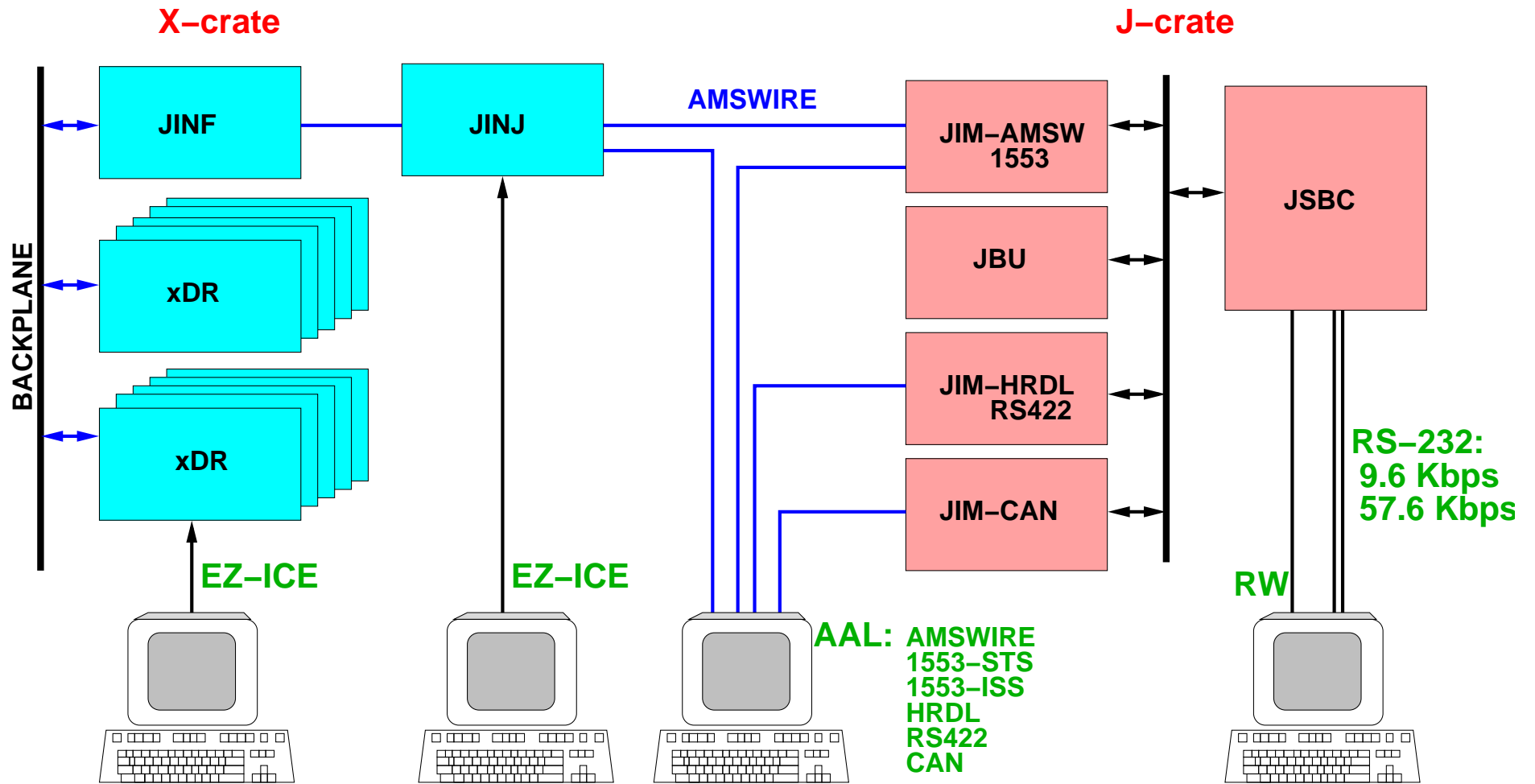
AMSW – LeCroy bus:

- control power supplies (HV, LV, DC/DC);
- control Solid State Fuses (Hot/Cold, multifunction).

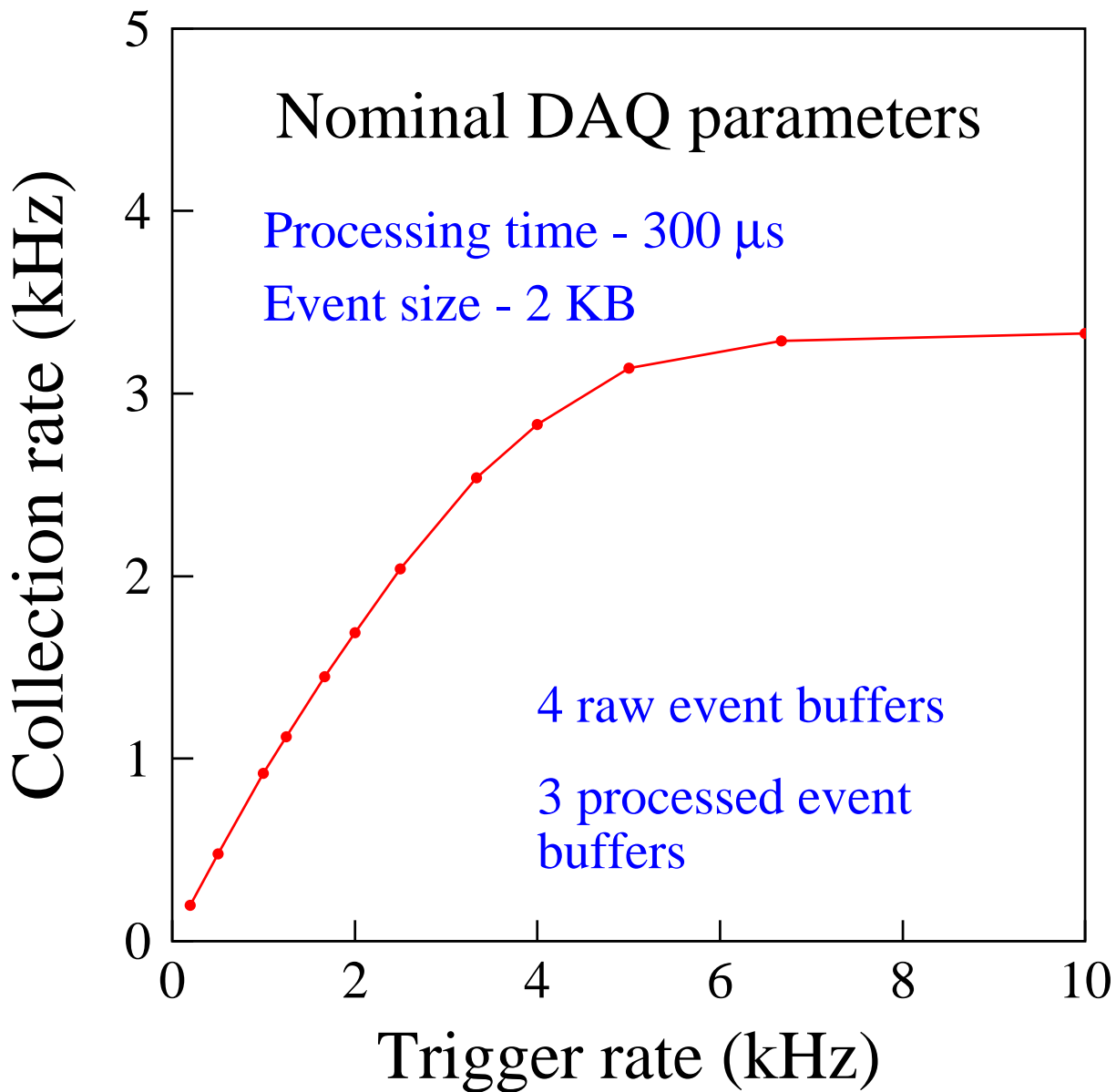
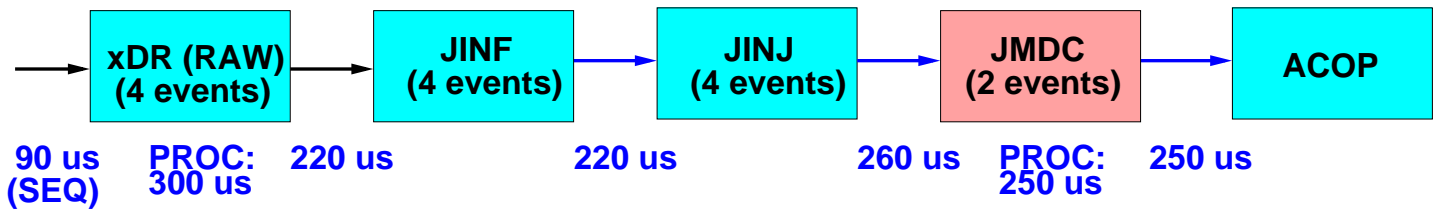
Voltage and Current monitoring:

- Acquires sensor readouts asynchronously;
- Stores this information locally;
- Provides this information to JINJ on request;
- Does not run some control algorithms.

Development setup



DAQ Performance - measurements



Hardware modifications

JINF modifications:

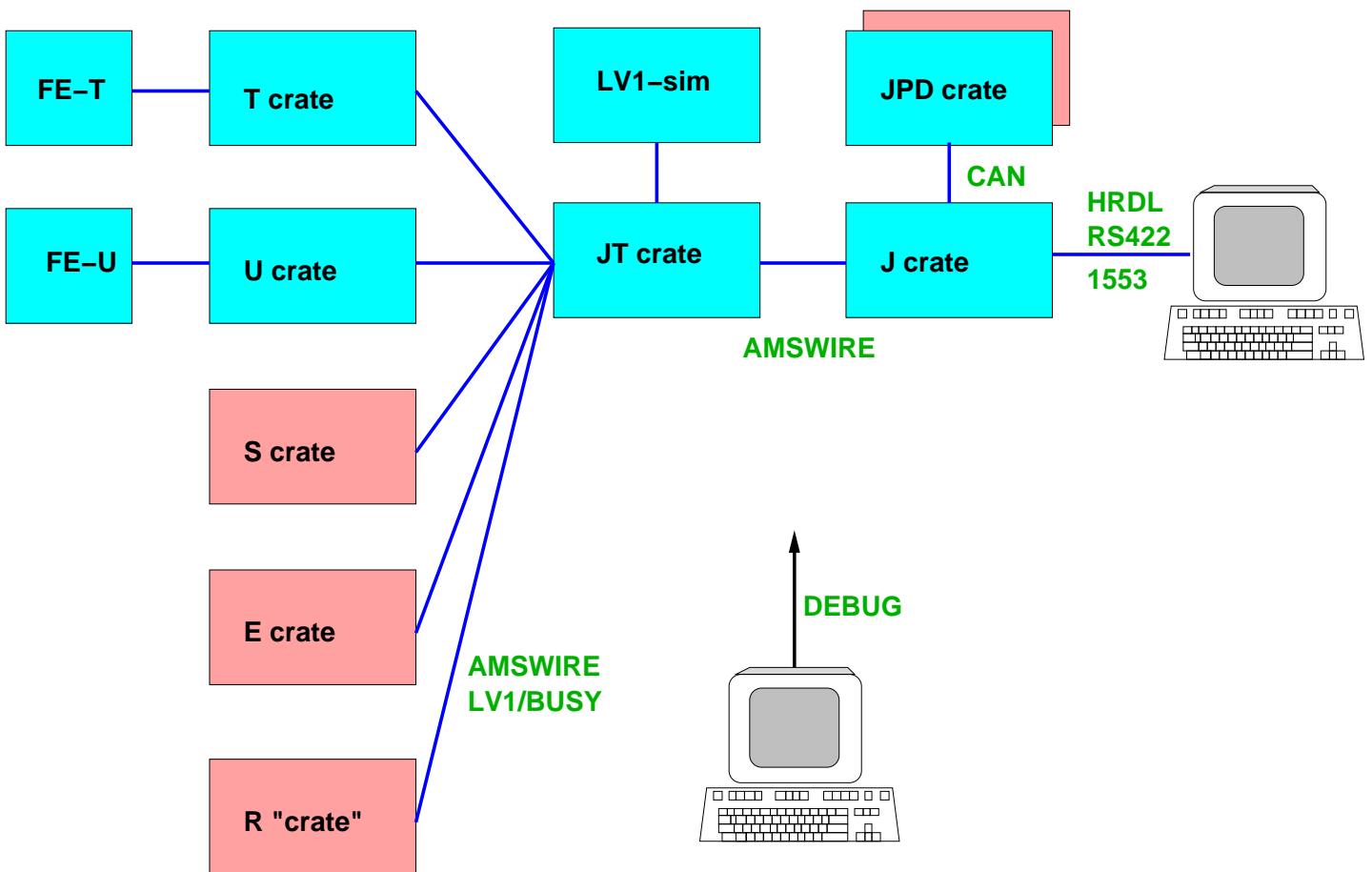
1. New functionality: Slow Control;
2. Test bench – new TBP, new JINF (+old TPSFE);
3. SW development pending HW availability (August 2004).

FLASH programming:

1. development of HW procedure;
2. rewriting protected FLASH sectors;
3. protecting FLASH sectors on-board.
4. Production: no programming before PCA.
5. FLASH programming is part of functional tests.

Plans

Goals for August 2004: assembly of TDR and UPR, JT, J, JPD crates commanded via 1553, HRDL/RS422 interfaces to PC.



Goals for November 2004 – March 2005: add missing parts.