

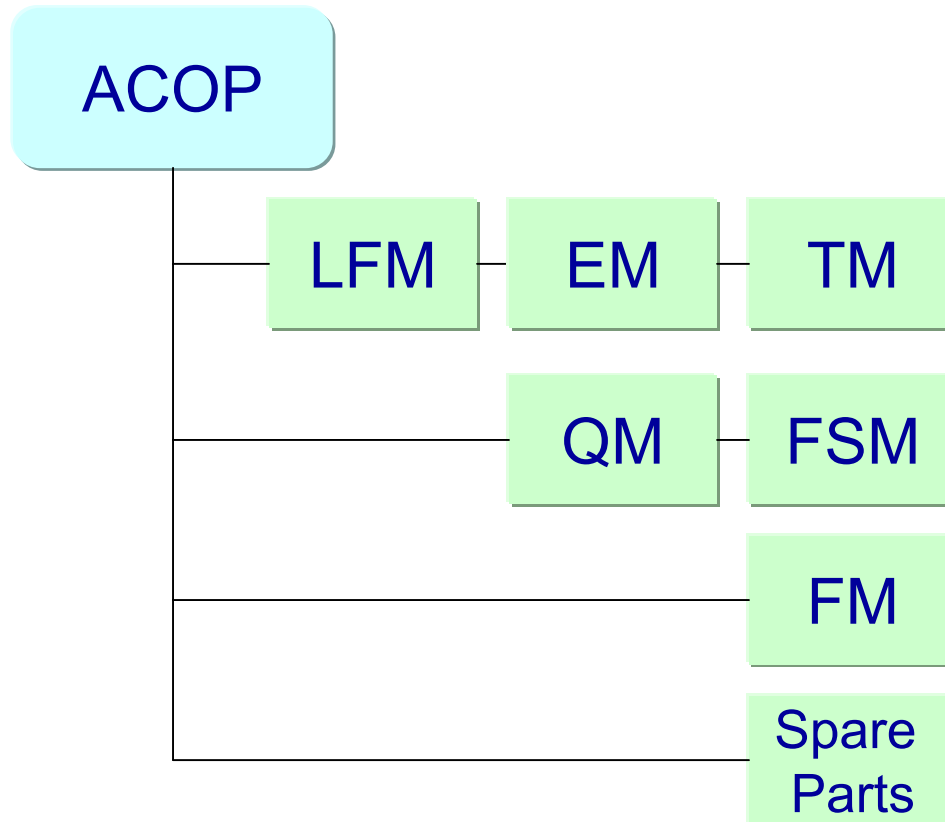
# ACOP: Agenda

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- ACOP models philosophy
- ACOP EXPRESS Rack accommodation
- ACOP ISO view new accommodation in the ISS Locker
- ACOP Electronics
- ACOP Electrical and Data I/F's
- ACOP SW Architecture
- ACOP Core
- ACOP ERLS Express Rack laptop computer
- ACOP LFM guidelines and architecture
- ACOP Status/Open Points

# ACOP: Models Breakdown

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- LFM Low Fidelity Model
- EM Engineering Model
- TM Training Model
- QM Qualification Model
- FM Flight Model
- Flight Spare Model
- Spare Parts and ORU

# ACOP: LFM/TM philosophy

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- **Low Fidelity Model**

- the LFM will be exploited to provide

- ACOP Software Development Environment (SDE)

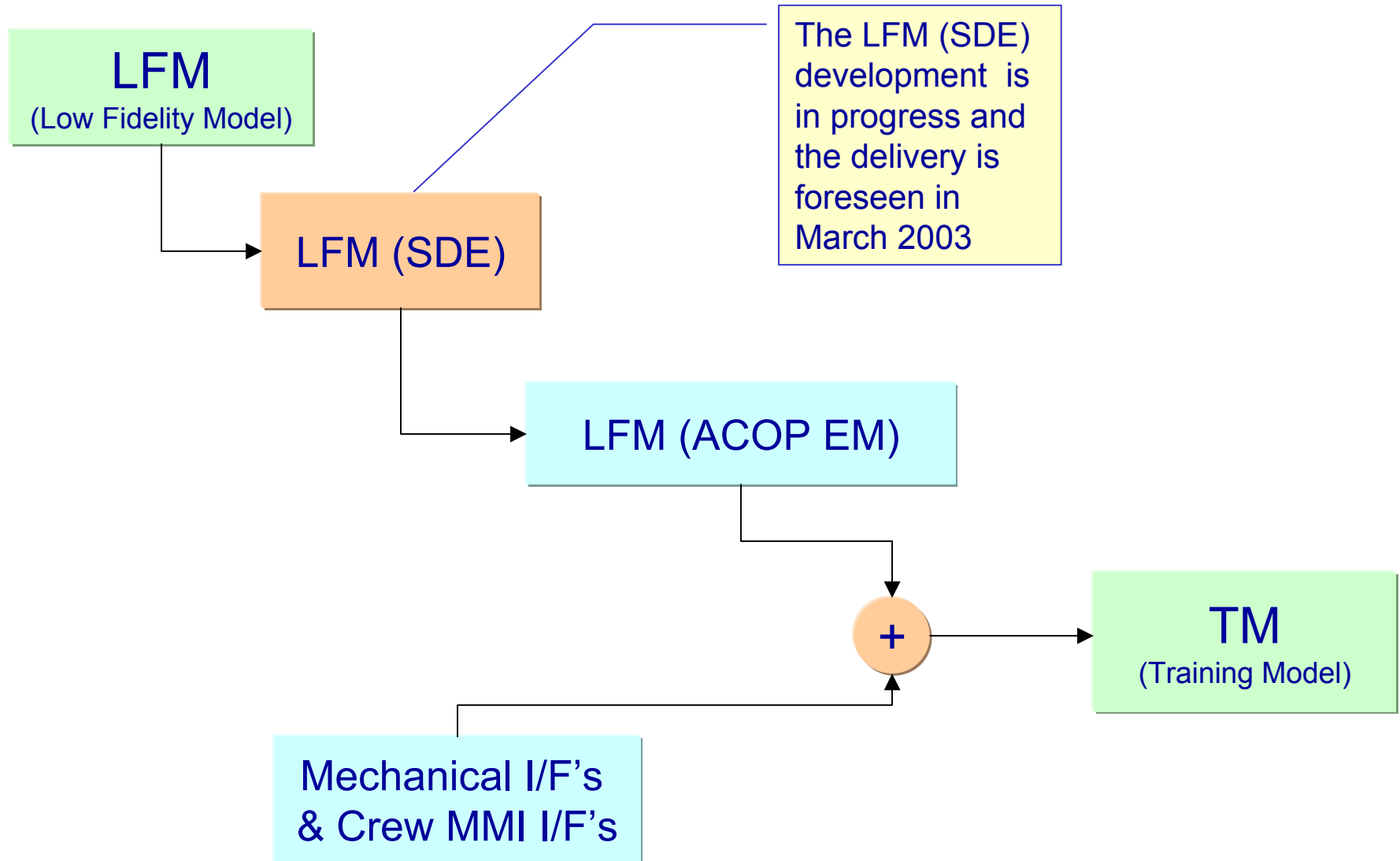
- ACOP Engineering Model (ACOP EM) - At the end of the SDE phase the LFM will be refurbished as required to be equivalent with the FM from a Electrical and Data management viewpoint.

- ACOP EM will be updated to become the Training Model

- **Training Model**

- Starting from the ACOP EM version it will be updated to become the Training Model (TM) by providing the required FM Mechanical Interfaces and Crew MMI interfaces.

# ACOP: LFM/TM transition schema



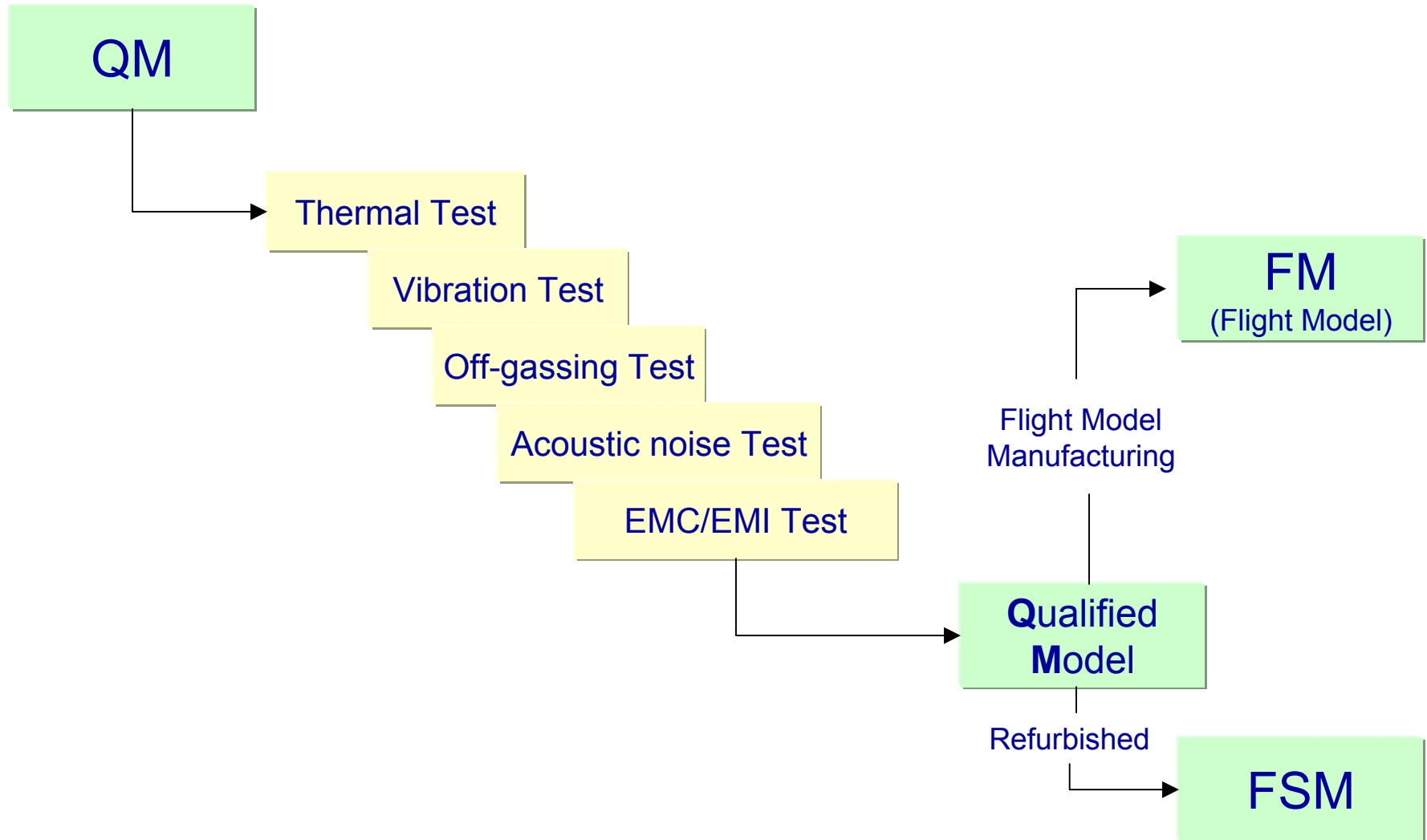
# ACOP: QM/FM/FSM

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- The Qualification Model is used during the Test phase and then it will be updated to Flight Spare Model.
  - The Qualification Model is the same replica of the ACOP Flight Model. It will be exploited during the test phase:
    - Vibration, Thermal, EMC, Materials, off-gassing, Acoustic
  - After the tests, the Qualification Model will be refurbished as required and will be available as Flight Spare Model (FSM).
  - The Flight Model is the model to be launched on orbit.

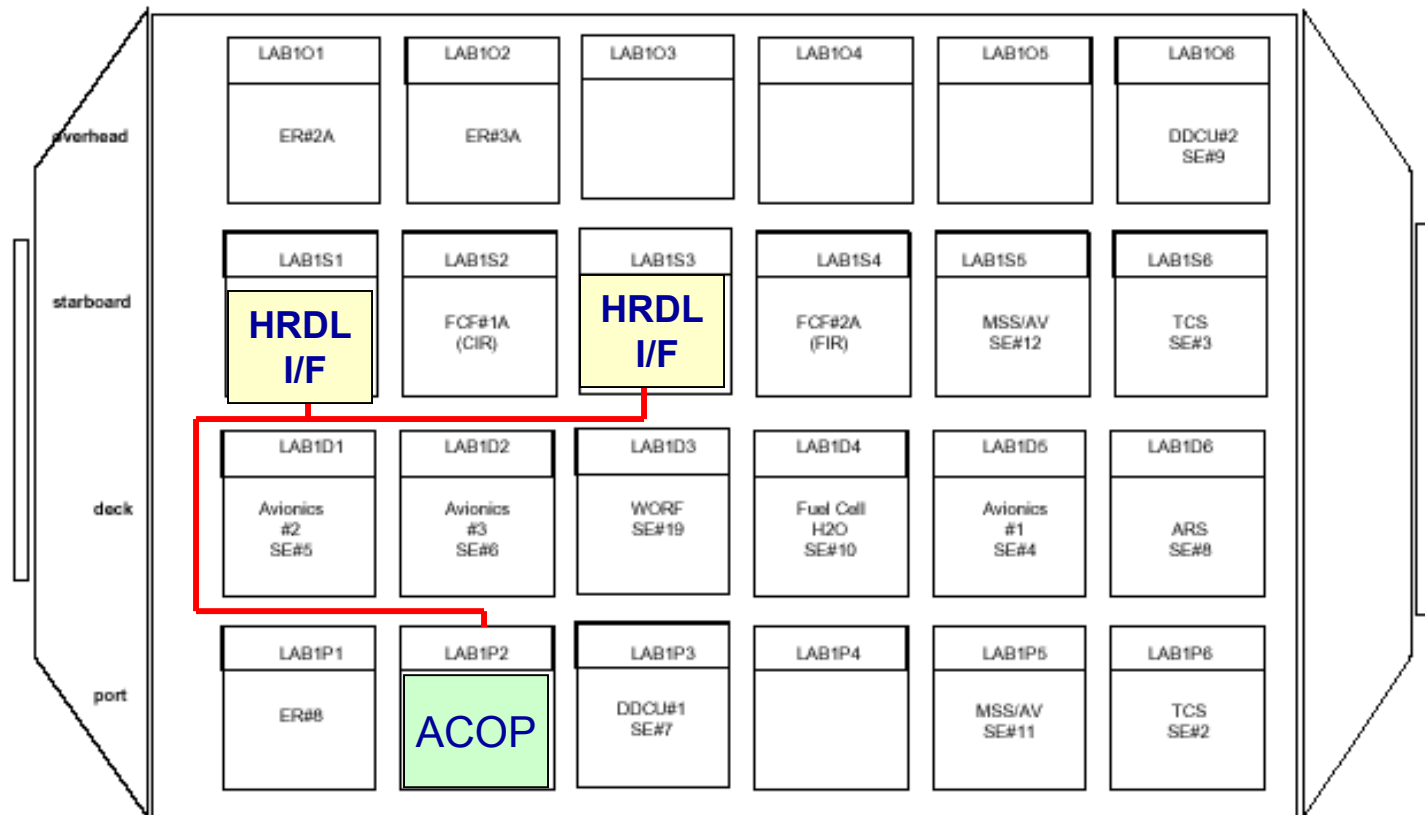
# ACOP: QM to FSM schema

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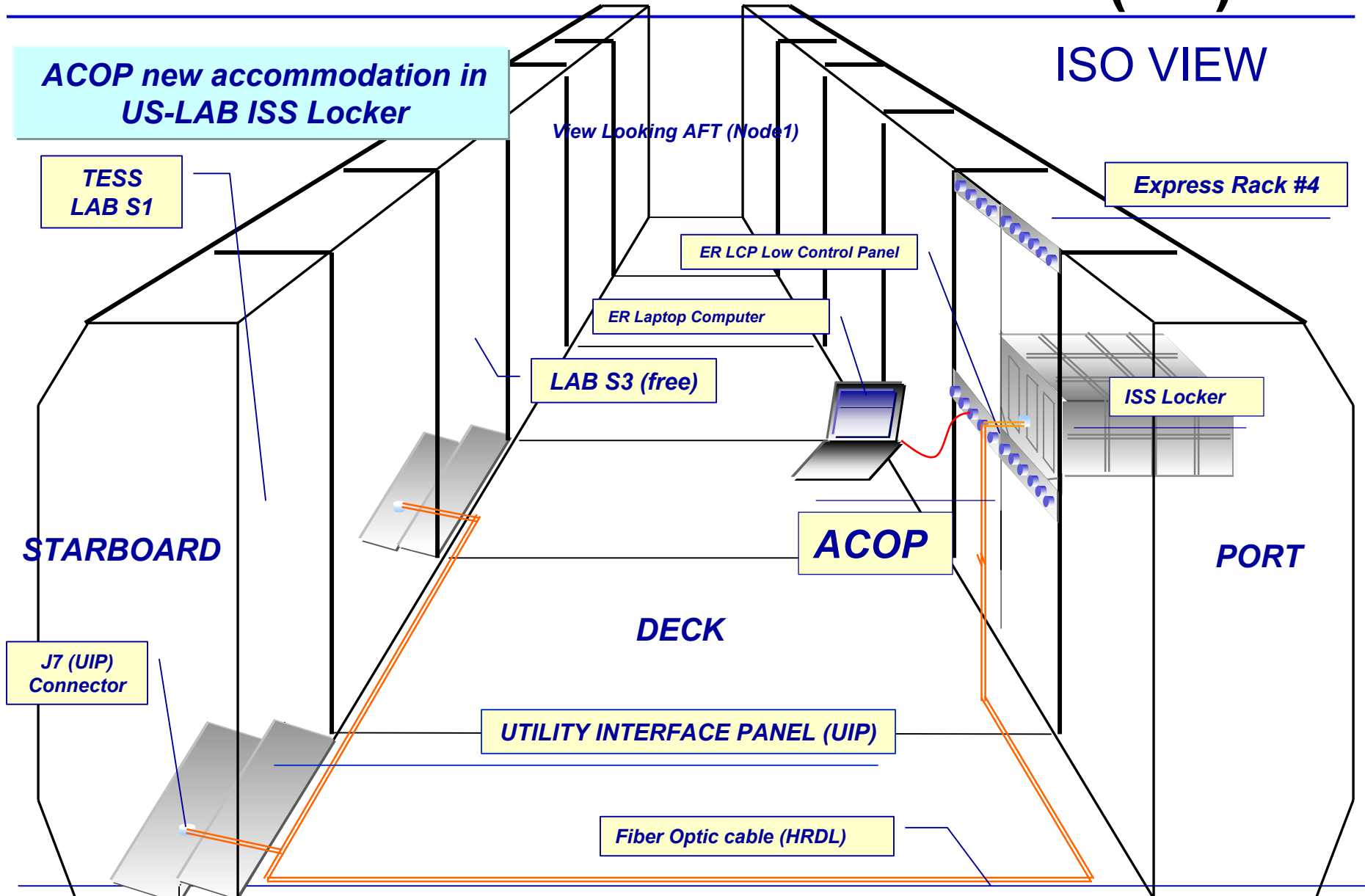


# ACOP: Us-lab Accommodation(1/2)

- ACOP is accommodated in a US-LAB Express Rack ISS Locker. Possible location available is LAB1P2 ER#4. HRDL connections available are LAB1S1 and LAB2S3

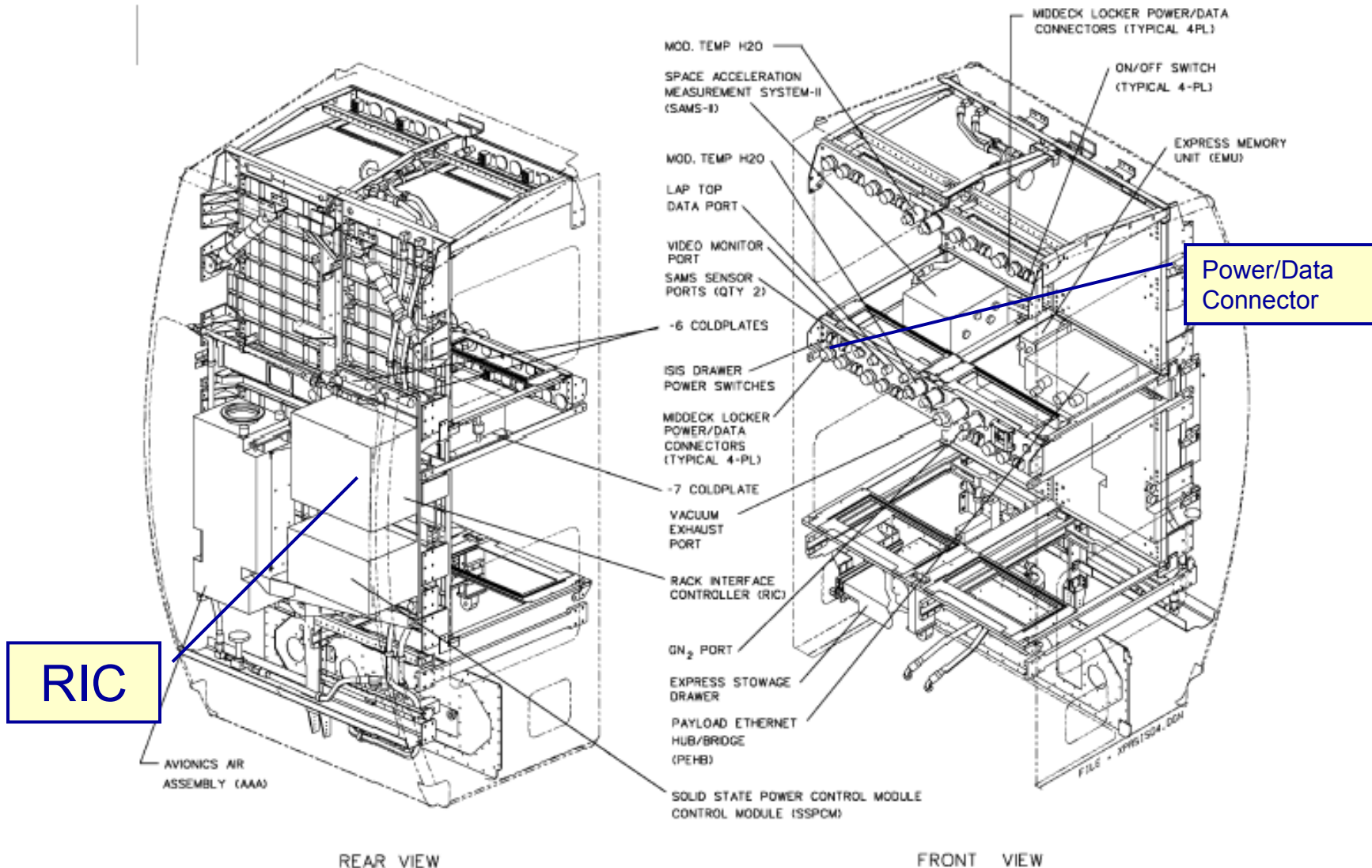


# ACOP: Us-lab accommodation (2/2)



# ACOP: ER accommodation (1/2)

## Express Rack architecture



RIC

Power/Data Connector

# ACOP: ER accommodation (2/2)



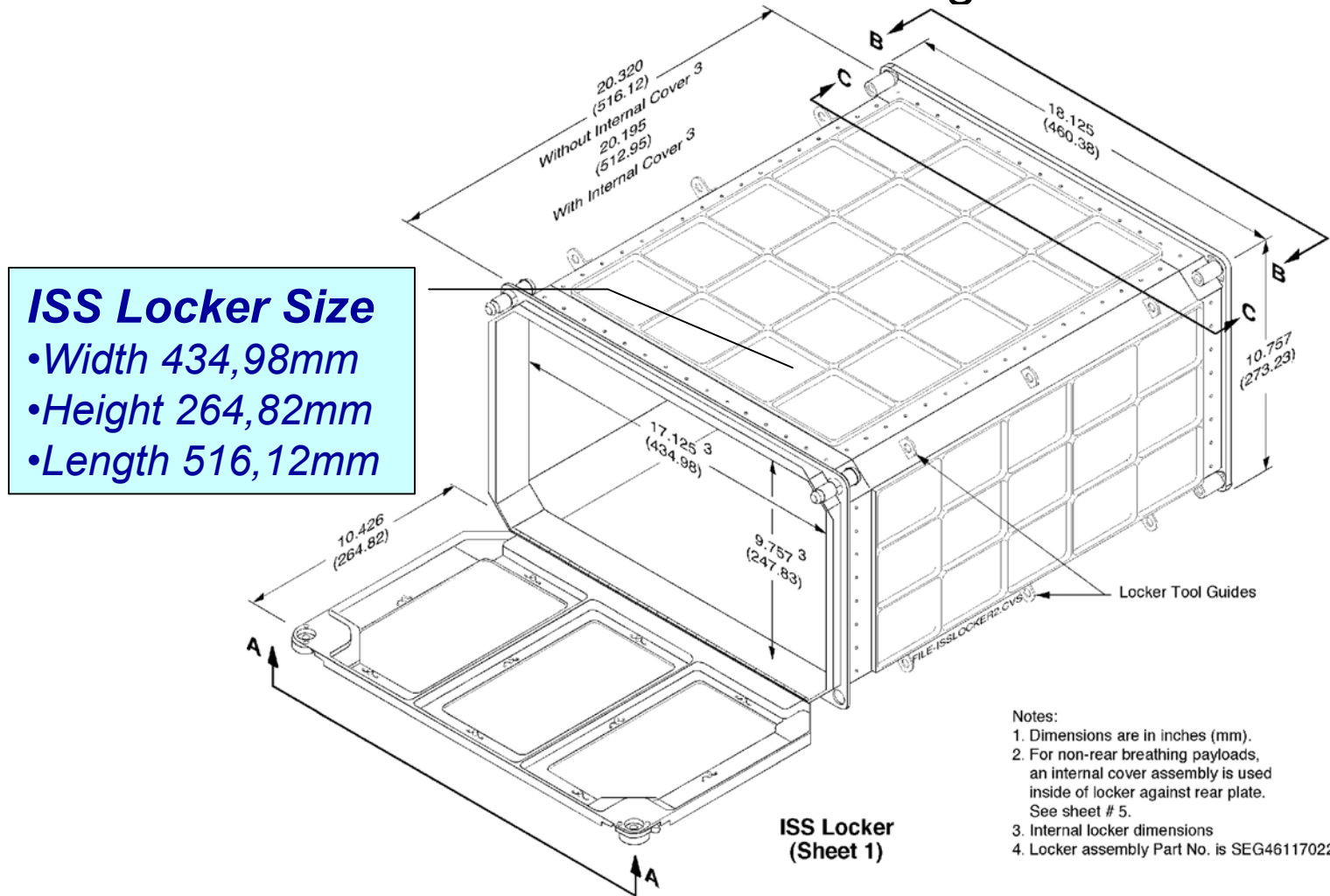
*ISS Locker available for ACOP in the ER#4*

*locker Power/Data Connector Panel (Power and data connector on ACOP front panel)*

*Another ISS Locker can be requested for ACOP ORU parts accom.*

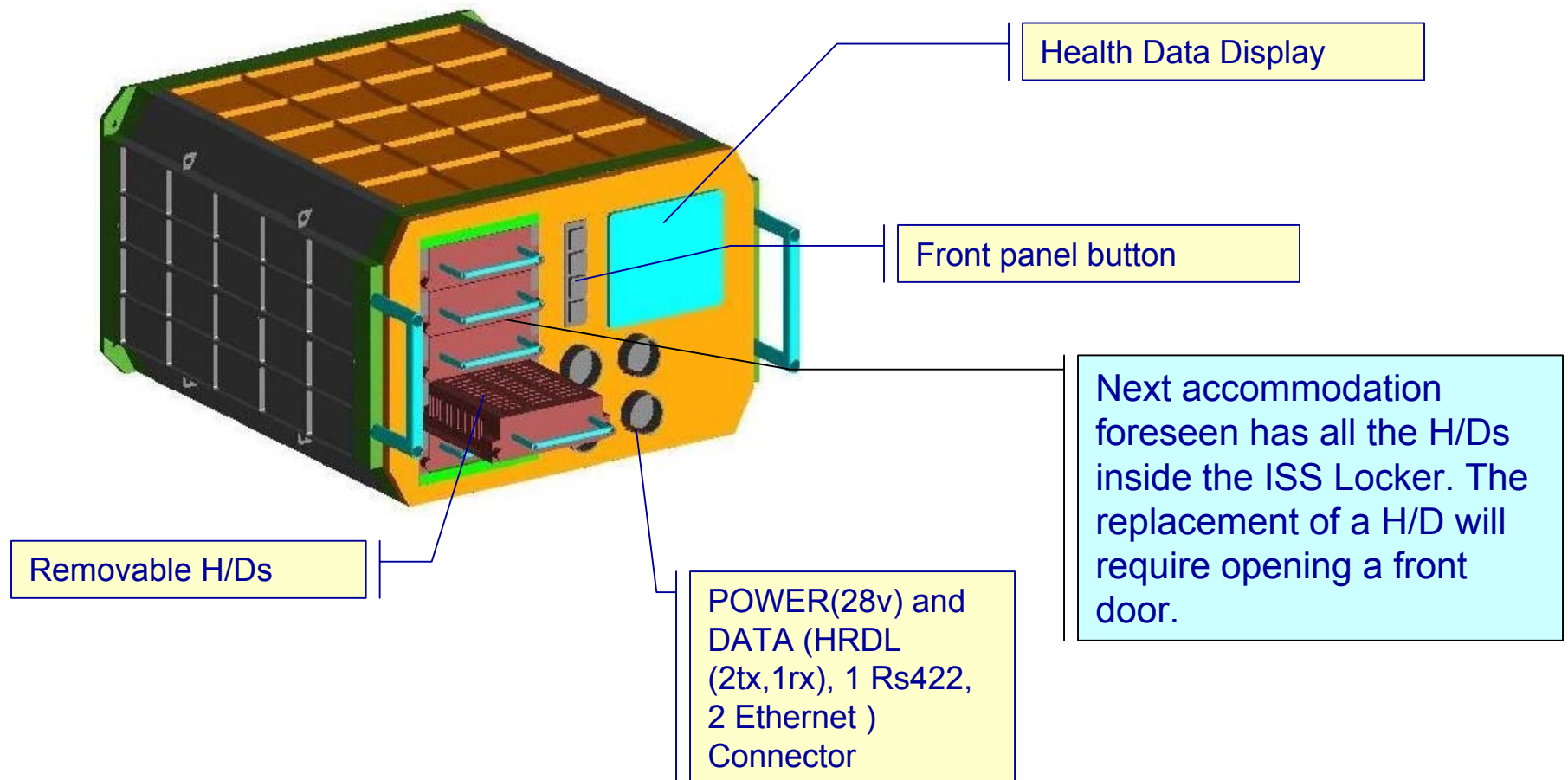
# ACOP: ISS Locker ISO view

- The slides shows an ISO view of a generic ISS locker



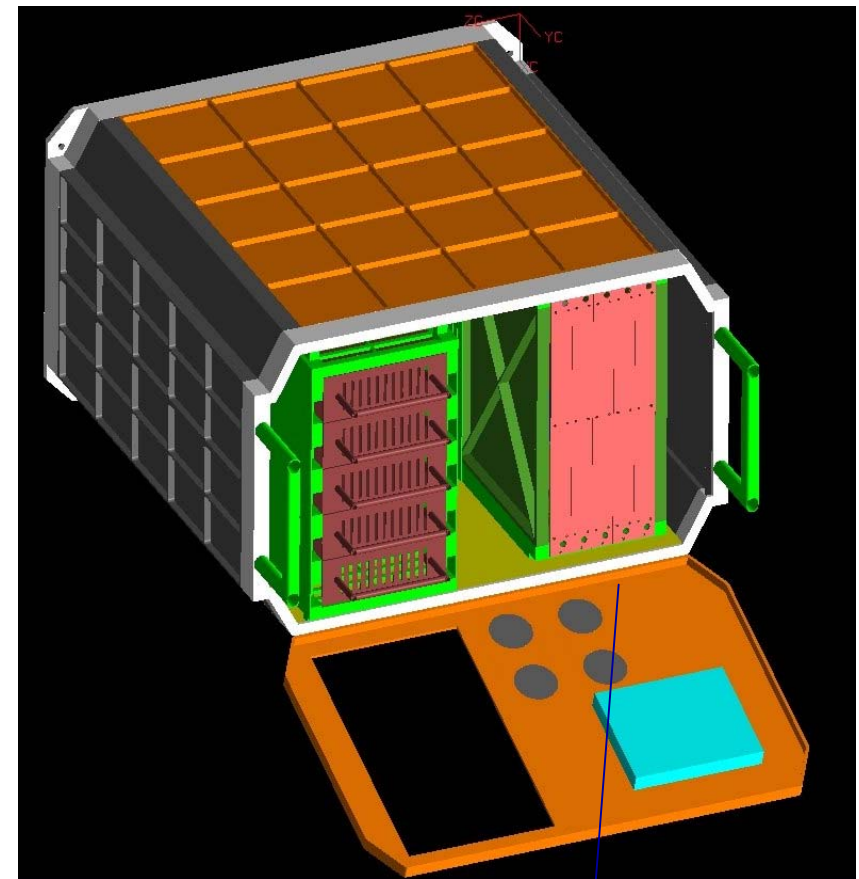
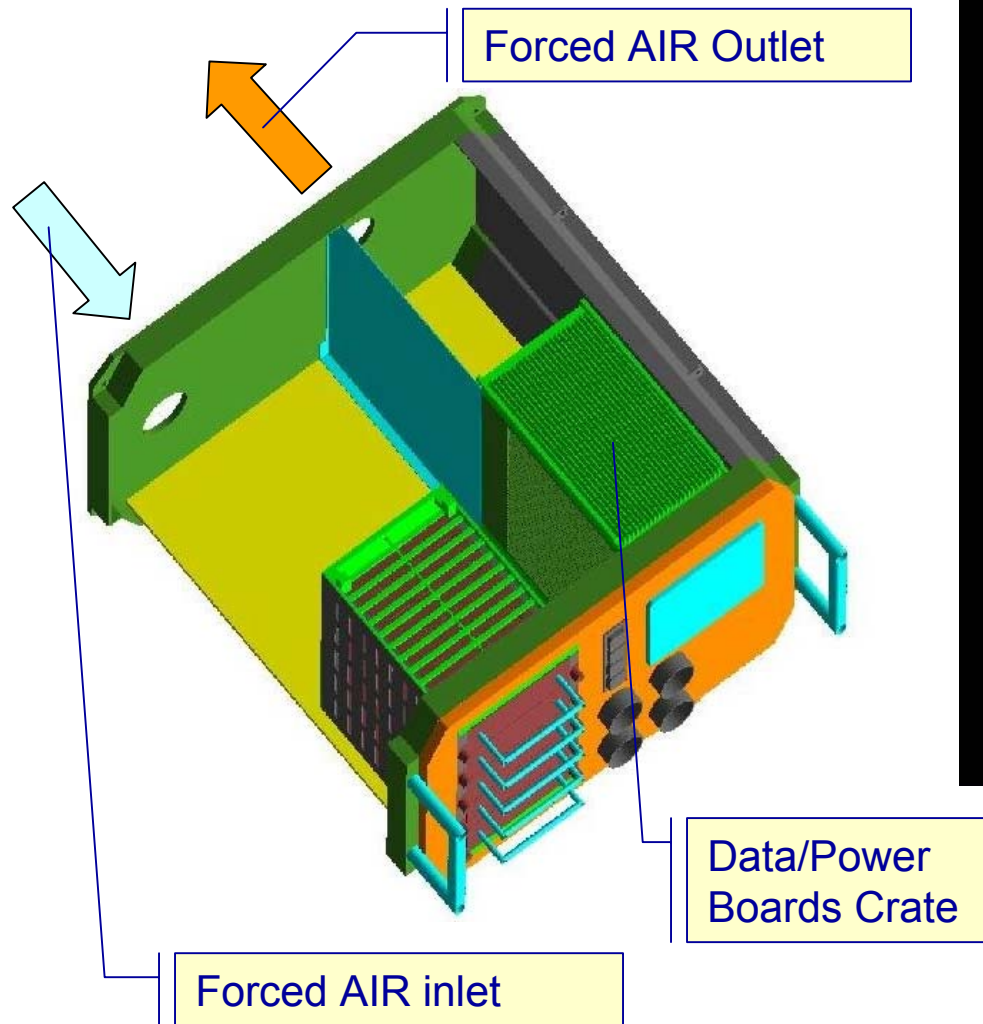
# ACOP: ACOP ISO view (1/2)

- The following slides show the preliminary design of ACOP inside an ISS locker

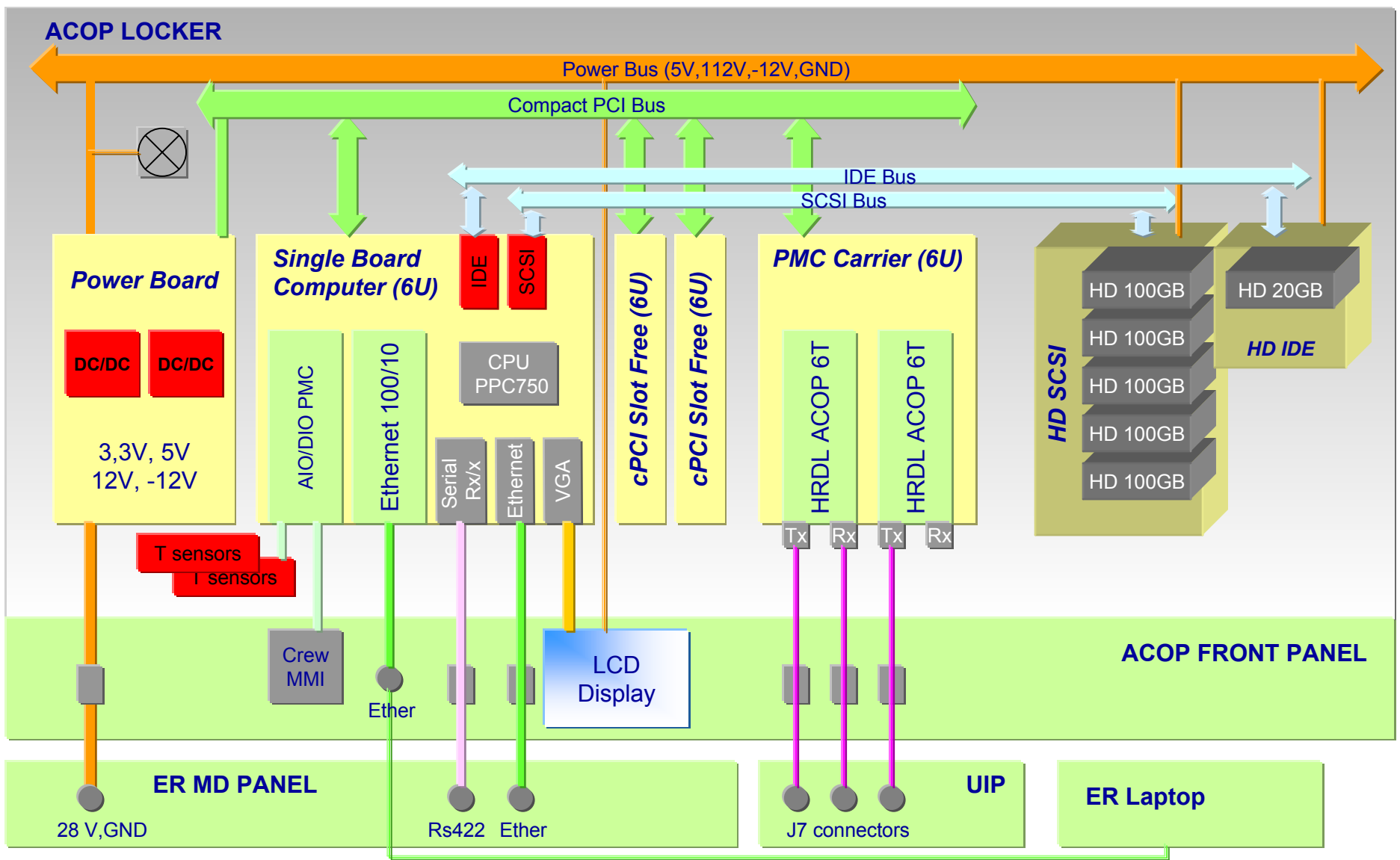


# ACOP: ACOP ISO view (2/2)

- ACOP Internal Layout



# ACOP: Electronic Baseline Schema



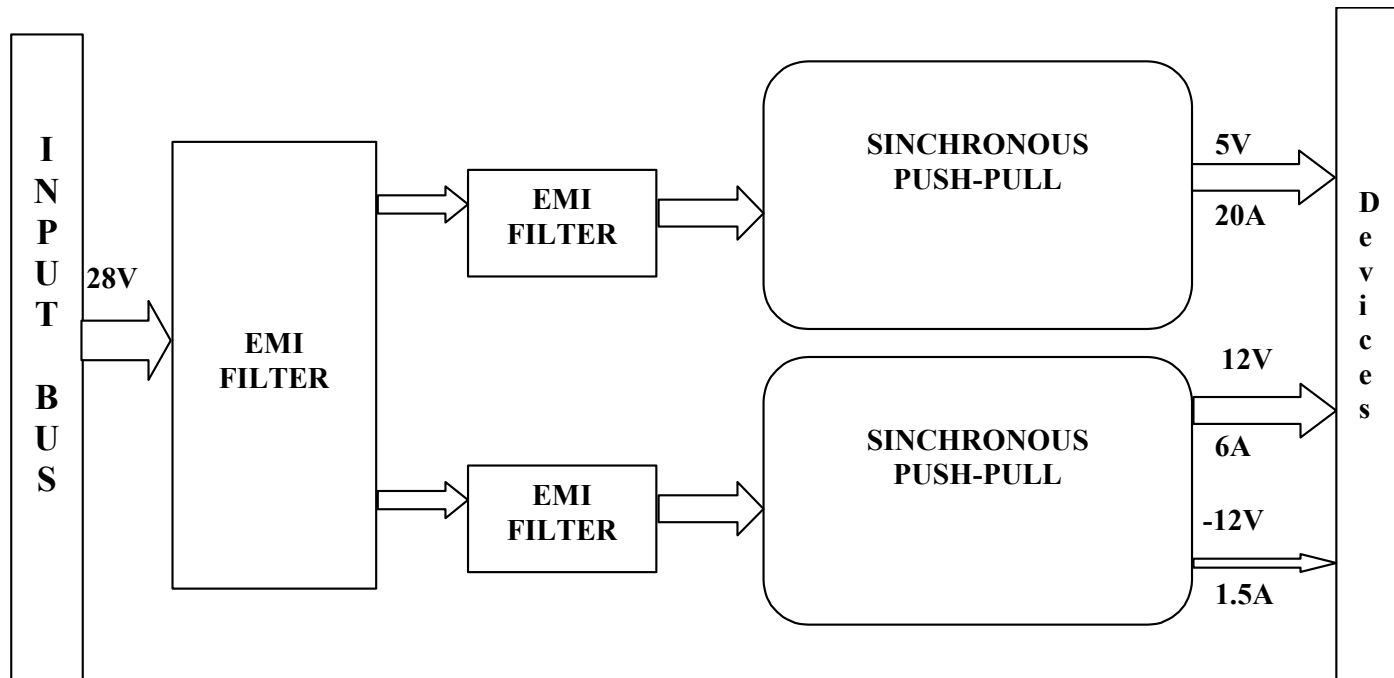
# ACOP: Electronic Components

<i>H/W</i>	<i>Provider</i>	<i>Remarks</i>
cPCI backplane	COTS	6U, with at least 4 available SLOT needed
Single Board Computer	COTS	CompactPCI 6U PowerPC 750 @ 400 MHz with 16MB flash, 1GB SDRAM, 512MB boot flash. No Conduction Cooling is required. No radiation tolerant is required. Ruggedized is required. Anyway will be selected boards that have different level of radiation tolerant
PMC Carrier Cards	COTS	As required . It depends on the number of controllers integrated (SCSI, IDE, ethernet...) and the number of available PMC slot on the processor board
Power Supply Board	CGS	Gives the requested power to cPCI BUS and to PWR Bus (3,3V, 5V,12V,-12V)
2 TAXI Optical Fiber PMC interface	CERN	ACOP 6T Board
I/O PMC card	COTS	Analog I/O to support internal Temperature monitoring and digital I/O to provide connections with buttons and controllers on the frontal Control Panel
Ethernet PMC card	COTS	Not needed if the main processor board provides two ethernet connections
IDE Hard Disk	COTS	The baseline foresees a solid state memory, but the possibility to mount an IDE disk will be evaluated
SCSI Hard Drive rack	COTS	Depending on the power and speed constraint can be replaced with high performance IDE devices. At least 500 Gbytes of storage capability
LCD display	COTS	320x240 color display

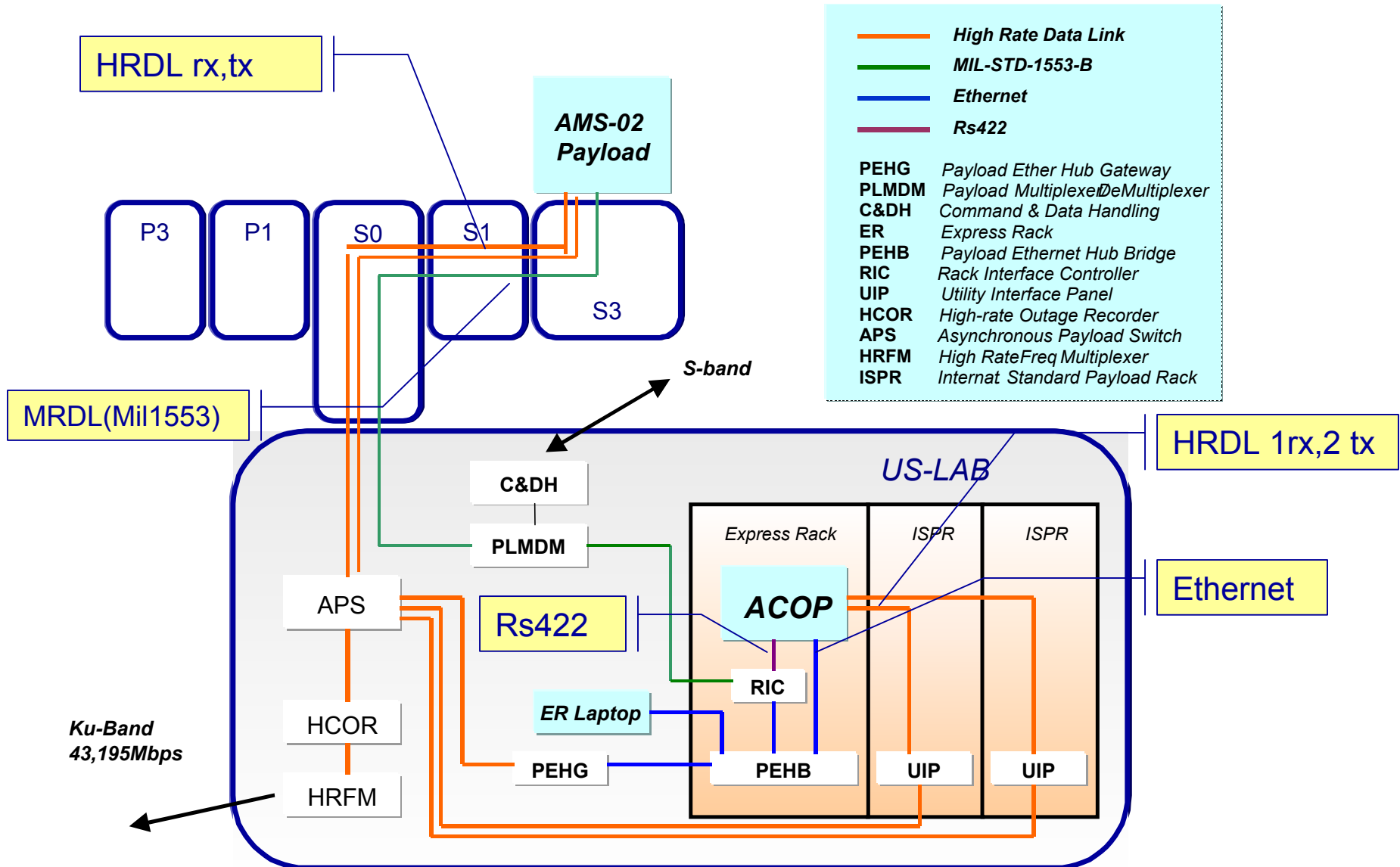
# ACOP: power board

Name	V <sub>out</sub> (V)	I <sub>out</sub> (A)	P <sub>out</sub> (W)
V1	5	20	100
V2	12	6	72
V3 opzionale	-12	1.5	18

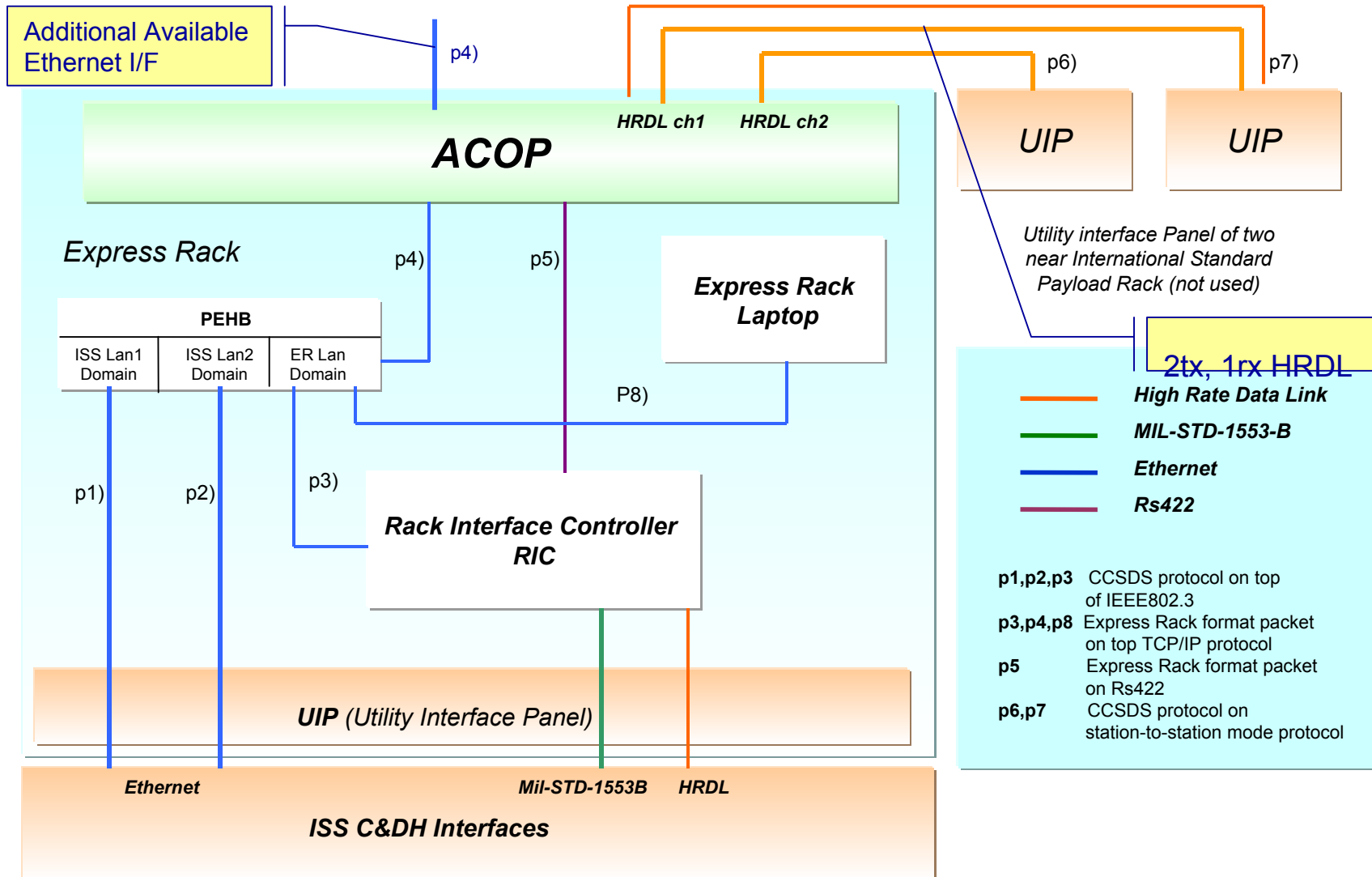
The Compact PCI Boards bus uses also a 3,3V. This outlet can be easily provided by using the following configuration through the synchronous push-pull. The total power provided will be the same decreasing the provided current by V1 outlet. The Power board is the only developed board



# ACOP: ISS Data I/F



# ACOP: Data I/F's



# ACOP: RIC Available Data packet

- RIC available data packet on Ethernet I/F. In the utilization column is defined the packet utilization in case of ACOP. The table is extracted from SSP52000-IDD-ERP

<b>Description</b>	<b>Source</b>	<b>Destination</b>	<b>Frequency</b>	<b>Data Format</b>	<b>Utilization</b>
<b>Ethernet Payload to RIC</b>					
Payload Health and Status	Payload	RIC	1Hz	Ethernet	Yes
PEP Bundle request	Payload	RIC	Async	Ethernet	No
PEP Procedure Execution Request	Payload	RIC	Async	Ethernet	No
Rack Time Request	Payload	RIC	Async	Ethernet	Yes
Ancillary Data Config Control	Payload	RIC	Async	Ethernet	Yes
Payload Telemetry Downlink Data	Payload	RIC	Async	Ethernet	Yes
EMU File Transfer Request	Payload	RIC	Async	Ethernet	No
Payload File Transfer Request	Payload	RIC	Async	Ethernet	Yes
Paylaod File Transfer Data Block	Payload	RIC	Async	Ethernet	No
<b>RIC to Ethernet Payload</b>					
Ancillary Data Set	RIC	Payload	Async, 0.1Hz,1H	Ethernet	Yes
Broadcast Ancillary Data Packet	RIC	Payload	10Hz	Ethernet	Yes
Rack Request response	RIC	Payload	Async	Ethernet	Yes
Rack Time Response	RIC	Payload	Async	Ethernet	Yes
EMU File Transfer Request	RIC	Payload	Async	Ethernet	No
Payload File Transfer Request	RIC	Payload	Async	Ethernet	No
Paylaod File Transfer Data Block	RIC	Payload	Async	Ethernet	Yes
Routed PEP Commands	RIC	Payload	Async	Ethernet	Yes

# ACOP:HRDL Available Data packet

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- On the Rs422 ACOP-RIC Interface are available the same data packet on Ethernet but for ACOP baseline the packet implementation is not foreseen.
- HRDL available data packet

<b>Description</b>	<b>Source</b>	<b>Destination</b>	<b>Frequency</b>	<b>Data Format</b>	<b>Utilization</b>
<b>ACOP to AMS-02</b>					
ACOP Commands	ACOP	AMS	Async	HRDL	Yes
File Transfer Upload	ACOP	AMS	Async	HRDL	Yes
<b>AMS-02 to ACOP</b>					
Command Response	AMS	ACOP	Async	HRDL	Yes
AMS Health & Status	AMS	ACOP	Async	HRDL	Yes
AMS Scientific Data	AMS	ACOP	20Mbps	HRDL	Yes
AMS House Keeping	AMS	ACOP	Async	HRDL	Yes

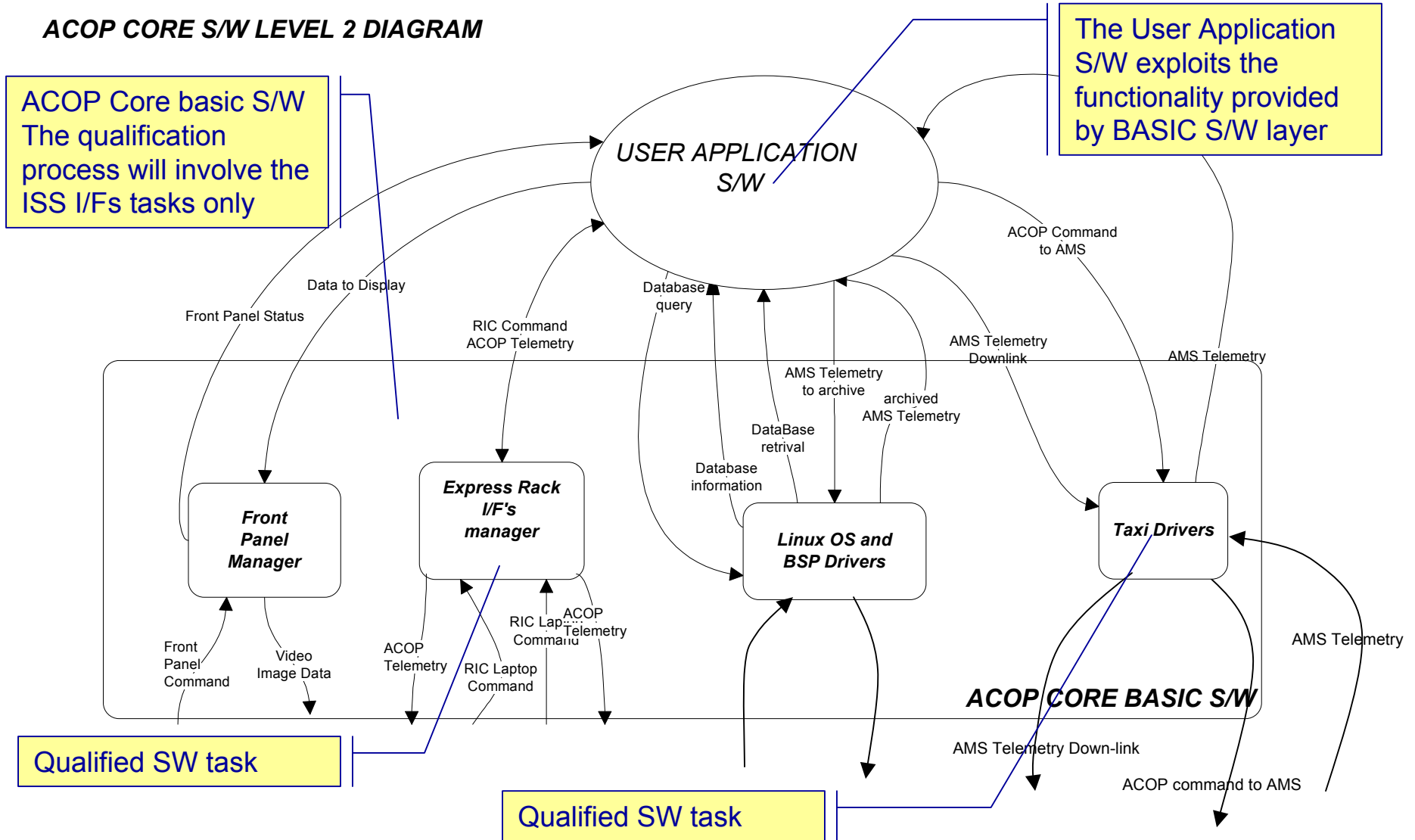
# ACOP: SW Breakdown

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- ACOP SW Breakdown
  - ACOP CORE S/W
    - ACOP CORE BASIC S/W
    - ACOP CORE USER APPLICATION S/W developed by CERN
  - ERLS (Express Rack Laptop Software) S/W
    - ERLS BASIC S/W
    - ERLS USER APPLICATION S/W developed by CERN

# ACOP: CORE SW CORE Top Level Architecture

ACOP CORE S/W LEVEL 2 DIAGRAM



# ACOP: LFM Development

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- The LFM model development is in progress and the LFM delivery as Software Development Environment is foreseen at the end of March 2002 before of the AMS CDR
  - The following top level requirements drives the LFM design
    - The LFM will be the ACOP Software Development Environment
    - The LFM will be an equivalent ACOP FM from a Data management viewpoint
    - The LFM will be used during the preliminary test of AMS (TBC)
    - The LFM will be update to a Training Model

# ACOP: Tasks to get the CDR

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- ISO View of ACOP in an ISS Locker
- Part/Components Selection frozen
- Power Schematics
- Engineering Drawings
- Express Rack / HRDL Interface Control Document
- Design Analysis report
- Software Interface Control Document
- EEE Parts Analysis
- Verification and Validation plan
- ORU parts list preparation and accommodation on ISS

# ACOP: Critical points

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- This is a list of Critical point to be discussed with NASA before the CDR in order to define and solve the following open points involving ACOP management and design.
  - High Rate Data Link Connection availability
  - Available Lockers / tray / Drawers in order to accommodate the ORU parts
  - Automated Payload Switching management w.r.t ACOP operation.
  - ACOP Launch date/Flight UF-5, UF-4