

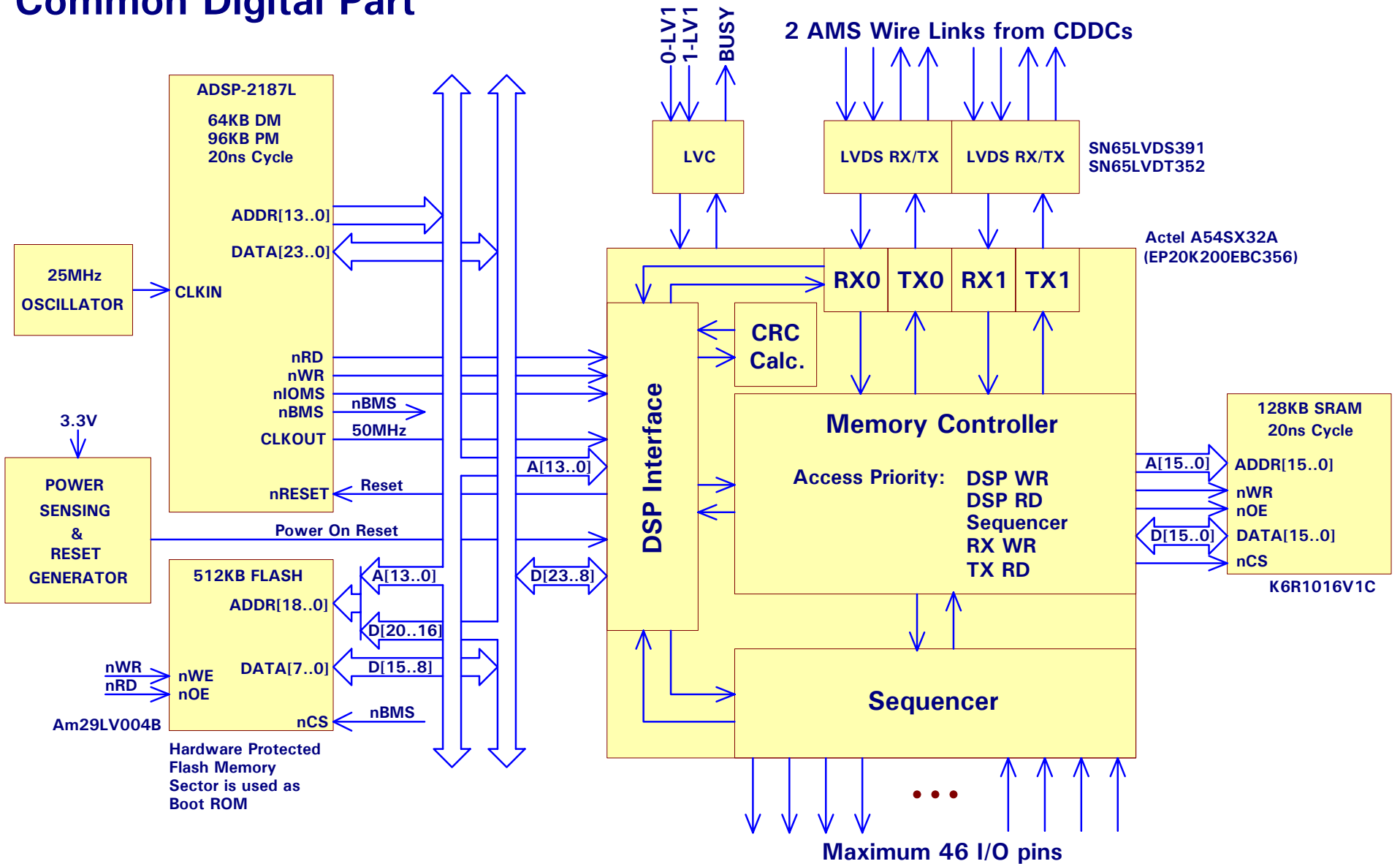
Common Digital Part (CDP): UDR,TDR,...

Command Distributor Data Concentrator (CDDC): JINF, JINJ

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AMS TIM Oct, 30 2002

Common Digital Part



Common Digital Part: Sequencer

(TDR Example)

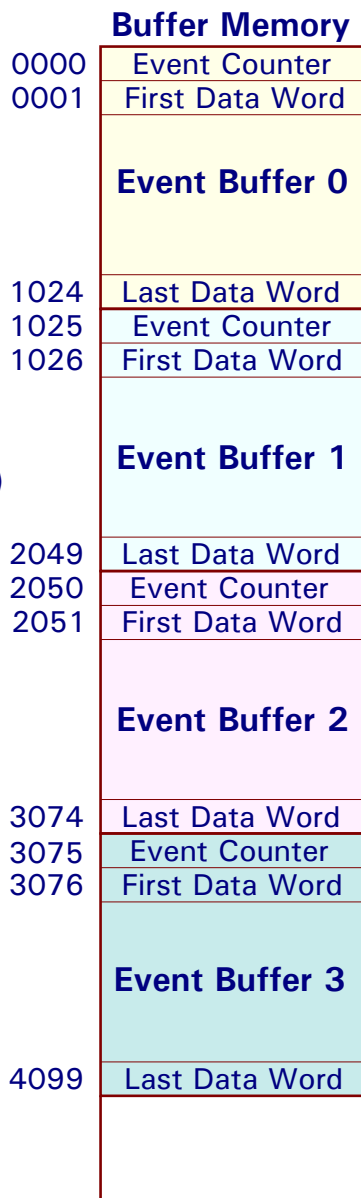
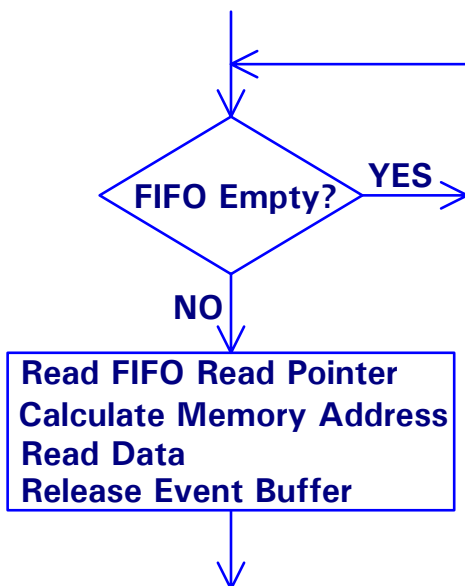
DSP has access to:

- 0 0** FIFO Read Pointer
- 1** FIFO Empty
- 0** Run
- 0** Busy

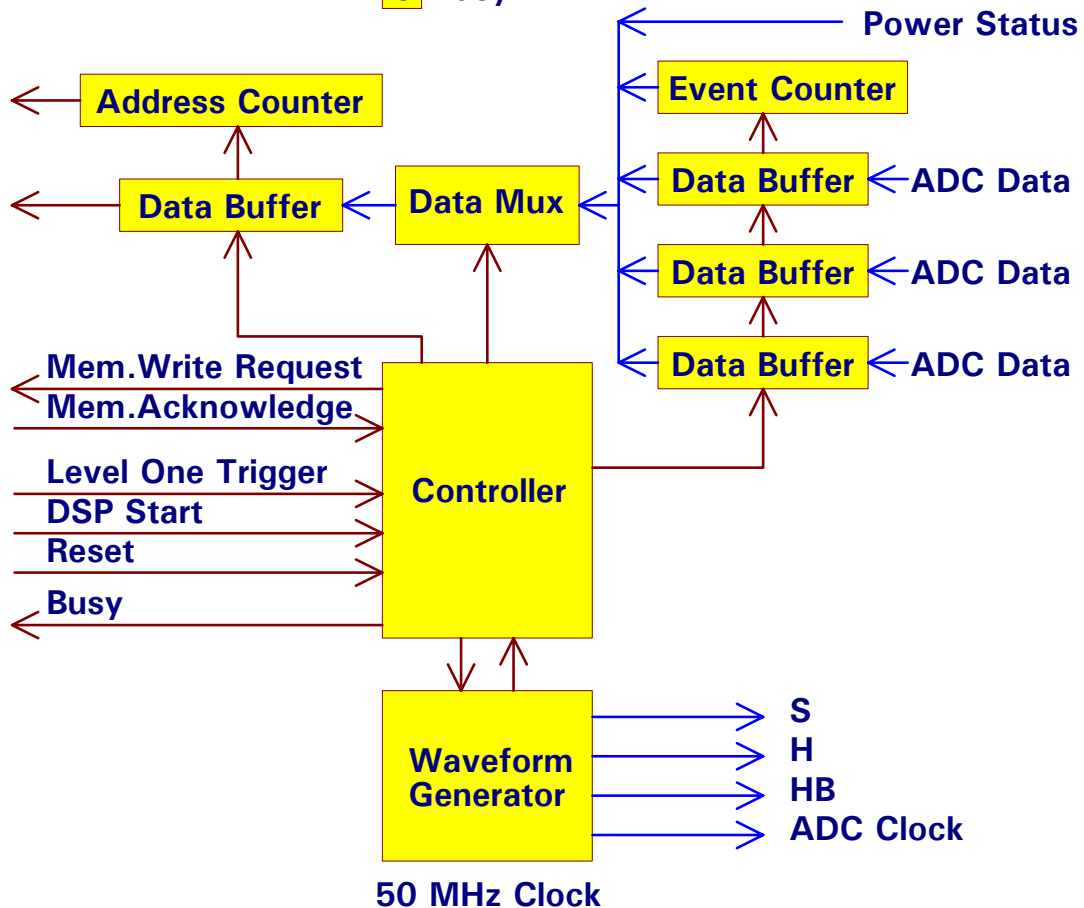
DSP can do:

- Reset Sequencer
- Release Event Buffer (Advance FIFO Read Pointer)
- Start Sequencer

DSP Read Event Procedure:



- 0 0** FIFO Write Pointer
- 0** FIFO Full
- 0** Run
- 0** Busy



Common Digital Part: Status

12 CDP Prototypes were made last year

CDP design was used to build TDR, UDR and LV1 EMs

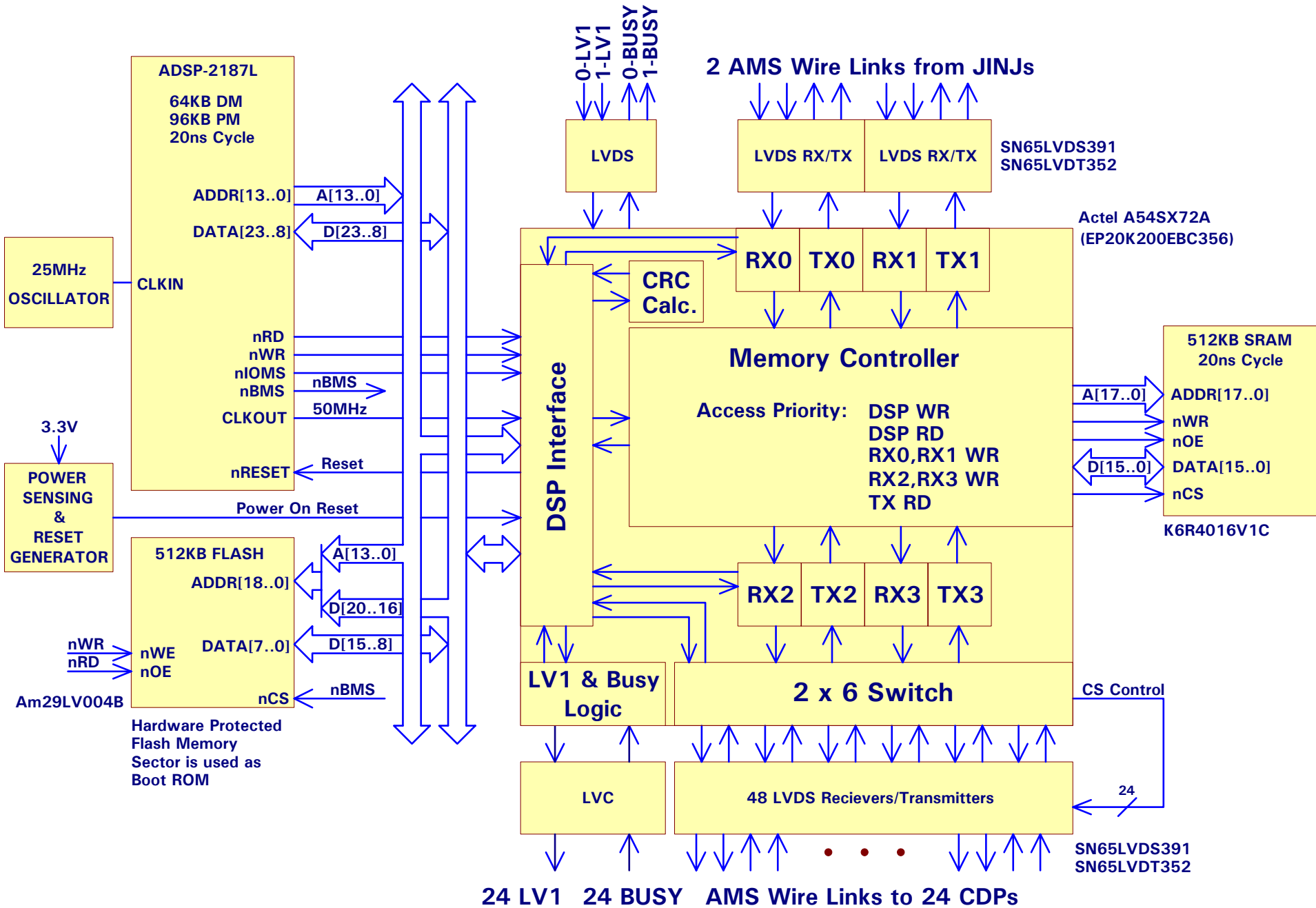
Sequencers for TDR and UDR are ready and tested

ACTEL version CDP prototype was made

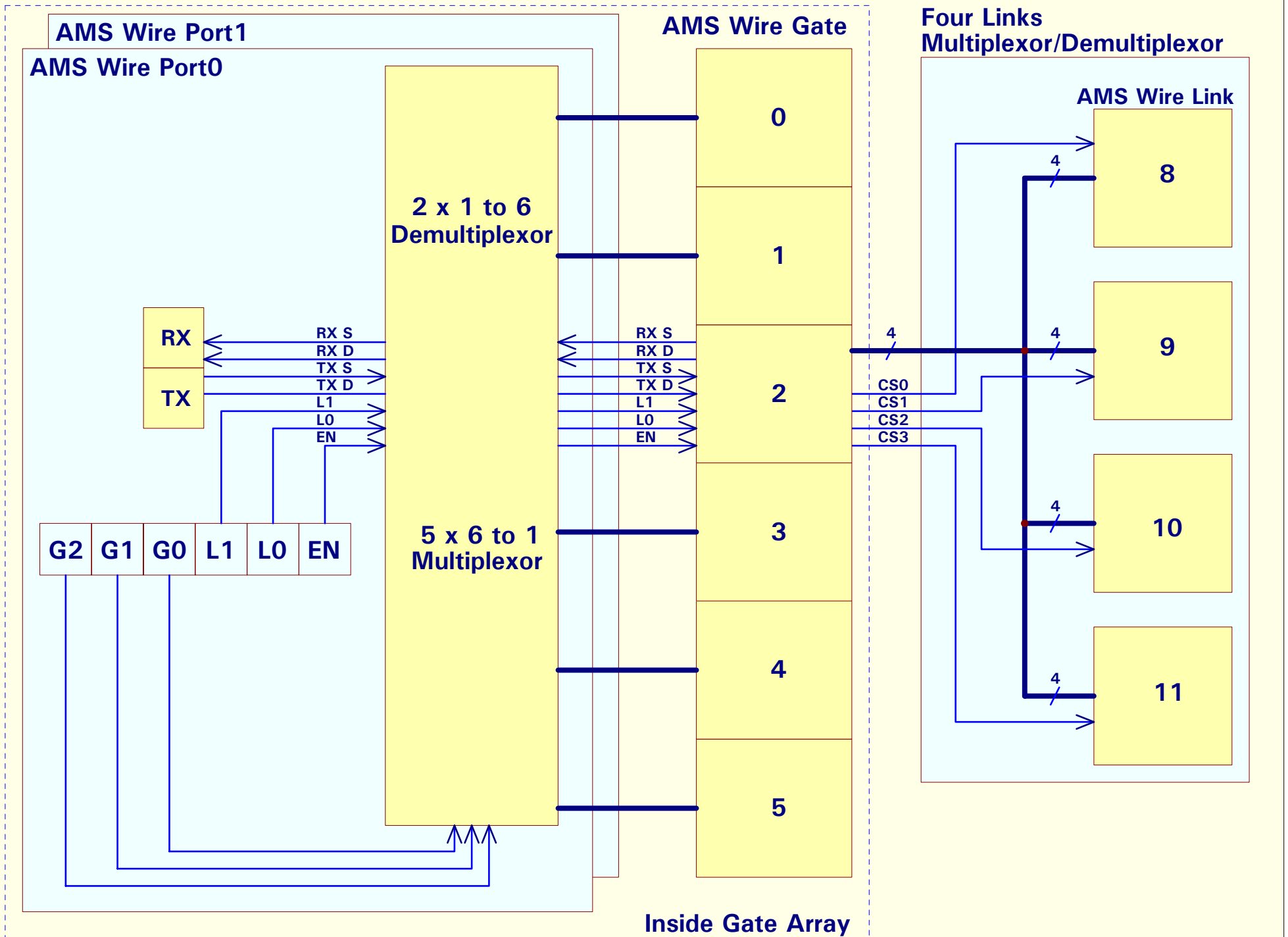
CAEN can proceed with TDR, UDR QM1

ECAL, RICH, TOF ?

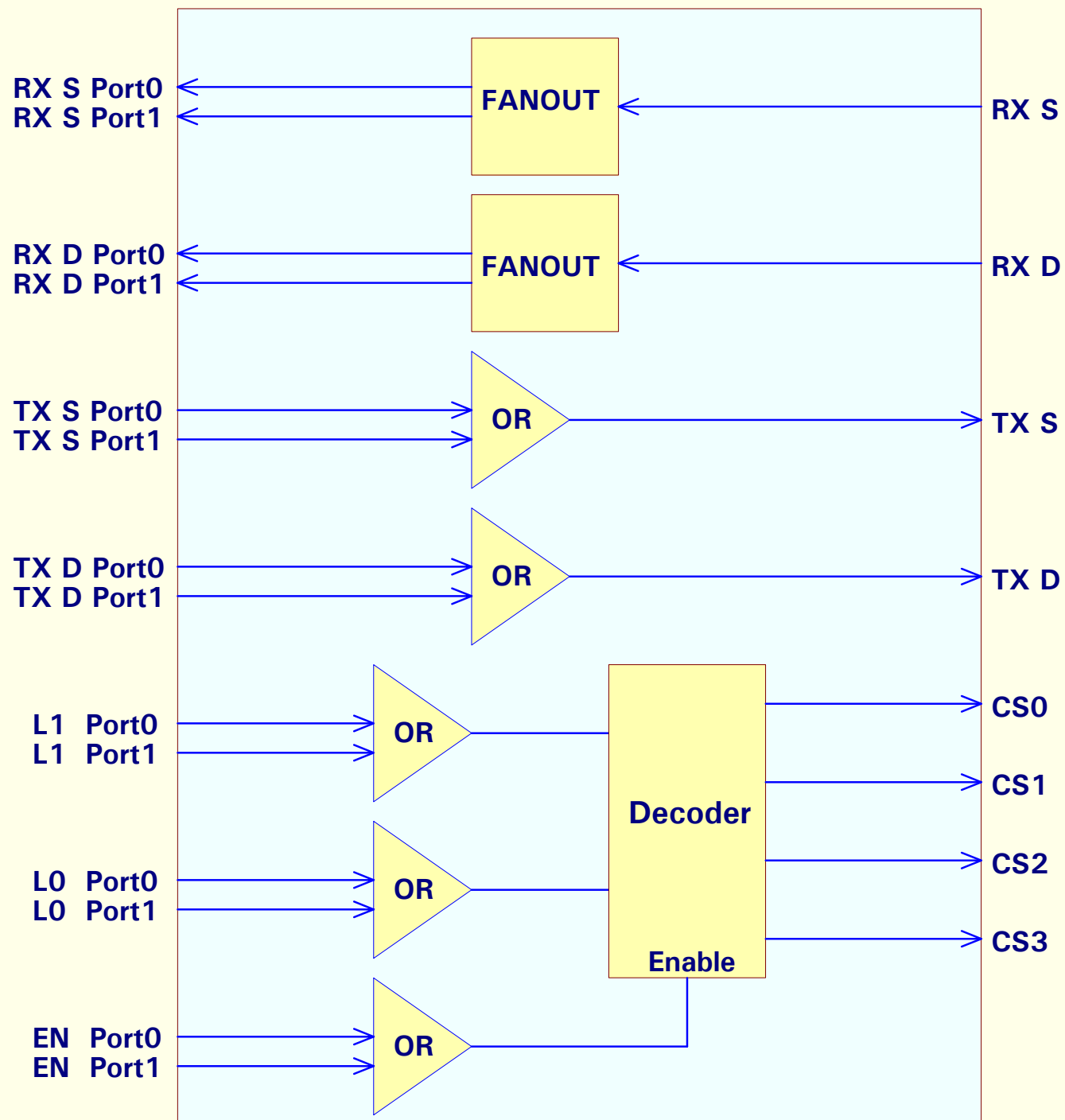
CDDC: JINF



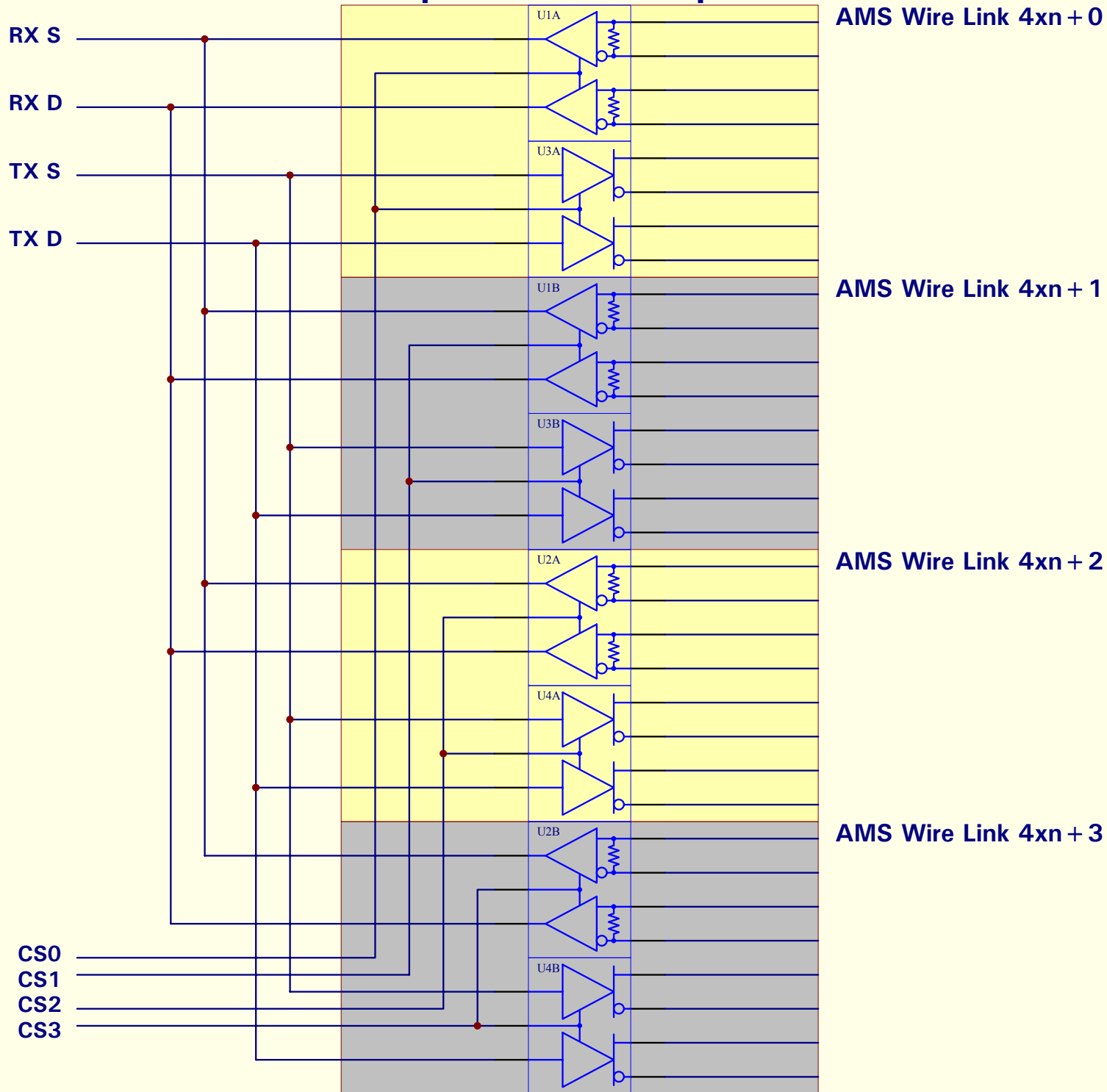
CDDC: 24 AMS Wire Links Multiplexor



CDDC: AMS Wire Gate



CDDC: Four AMS Links Multiplexor/ Demultiplexor



CDDC JINF: Status

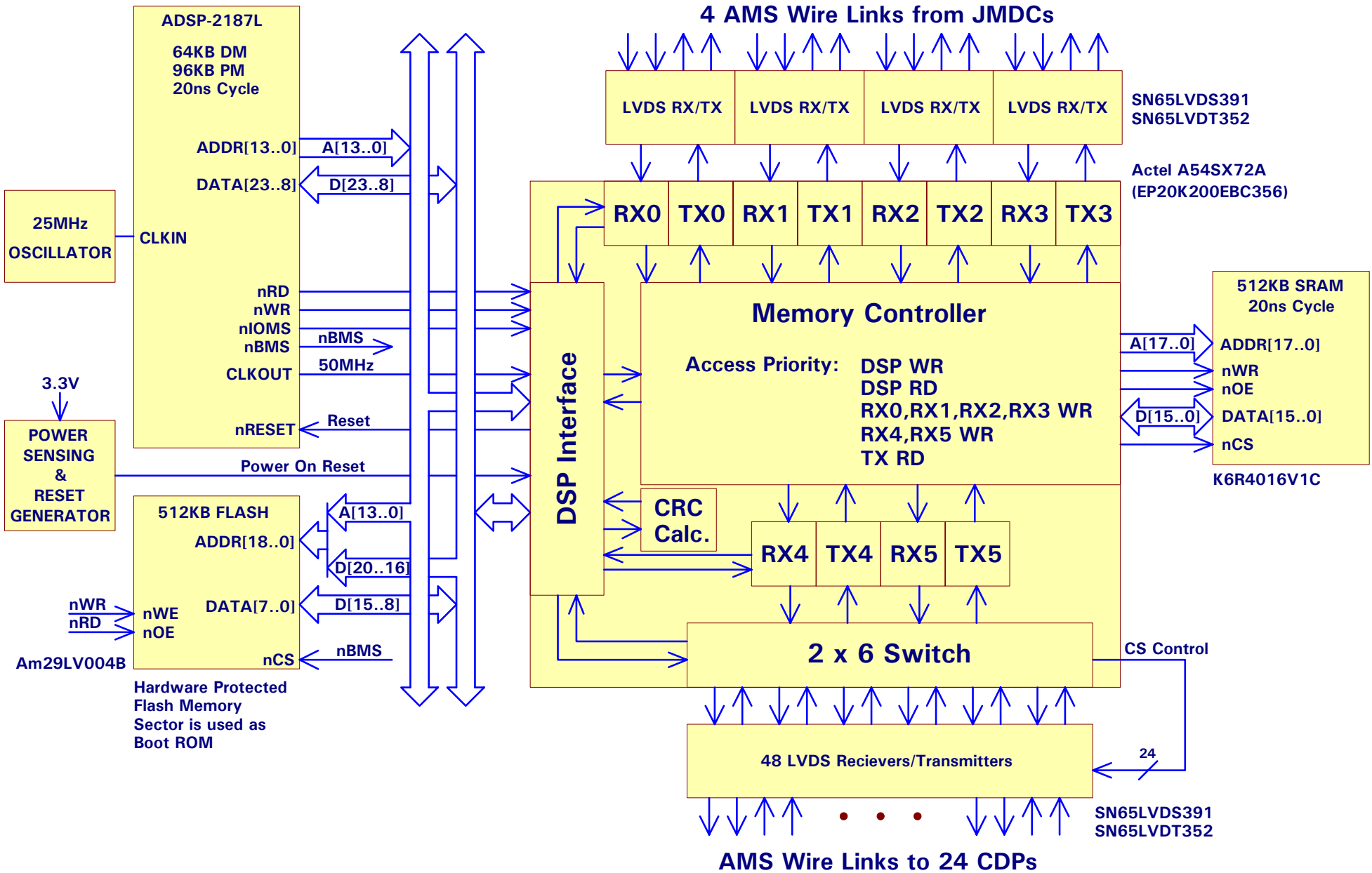
JINF Prototype was made last year

First version FPGA design was made April 2002

JINF EM board design is ready (ACTEL)

Two JINF EMs will be made at CERN

CDDC: JINJ



CDDC JINJ: Status

JINJ Schematics are ready (ACTEL)

JINJ PCB design will be ready at Jan 2003