



Status Report for AMS Trigger System

AMS DAQ Group



Outline

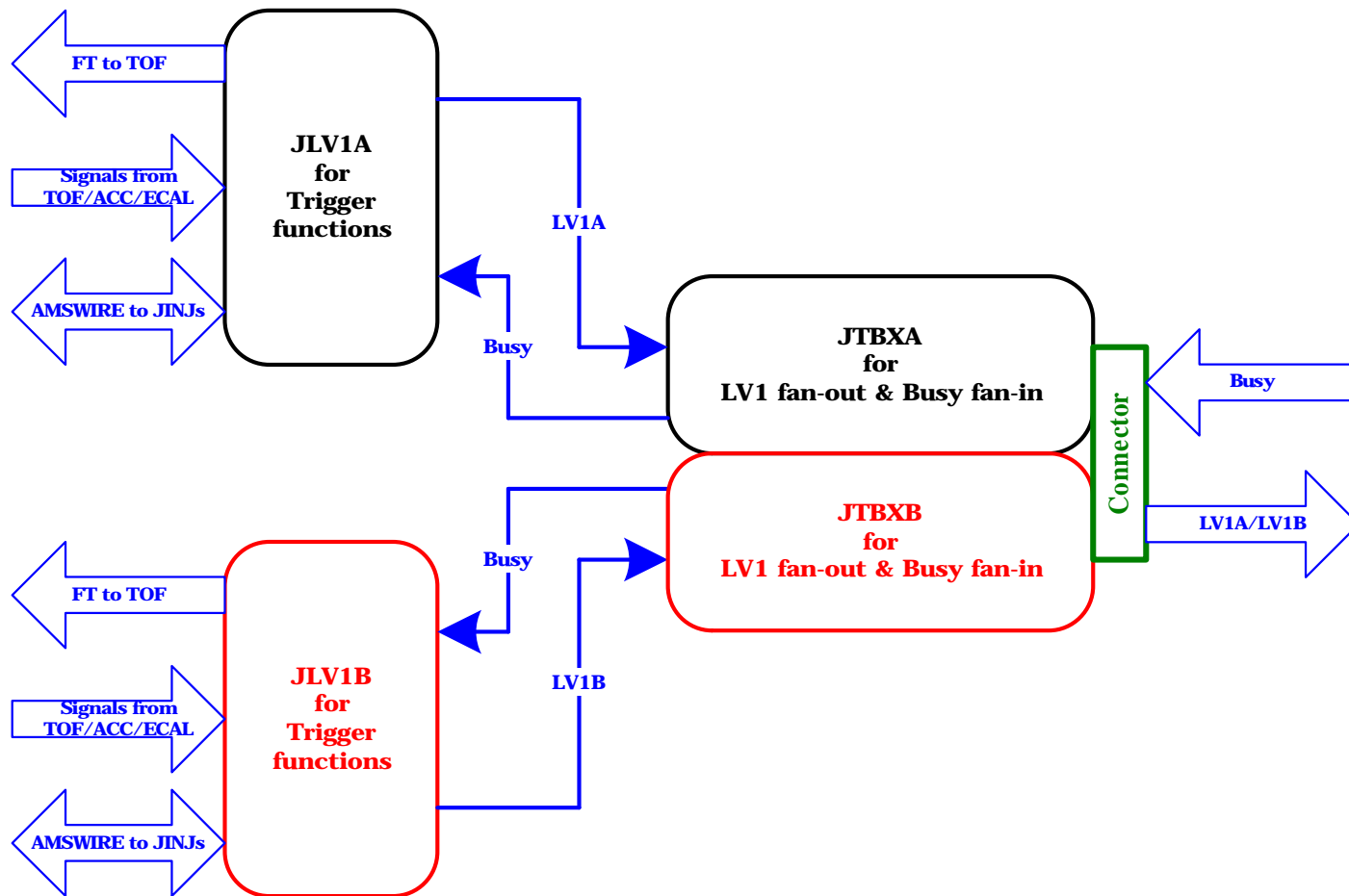
- Introduction
 - Requirement
 - Block Diagram
- JLV1 Design
- JTBX Design
- Schedule



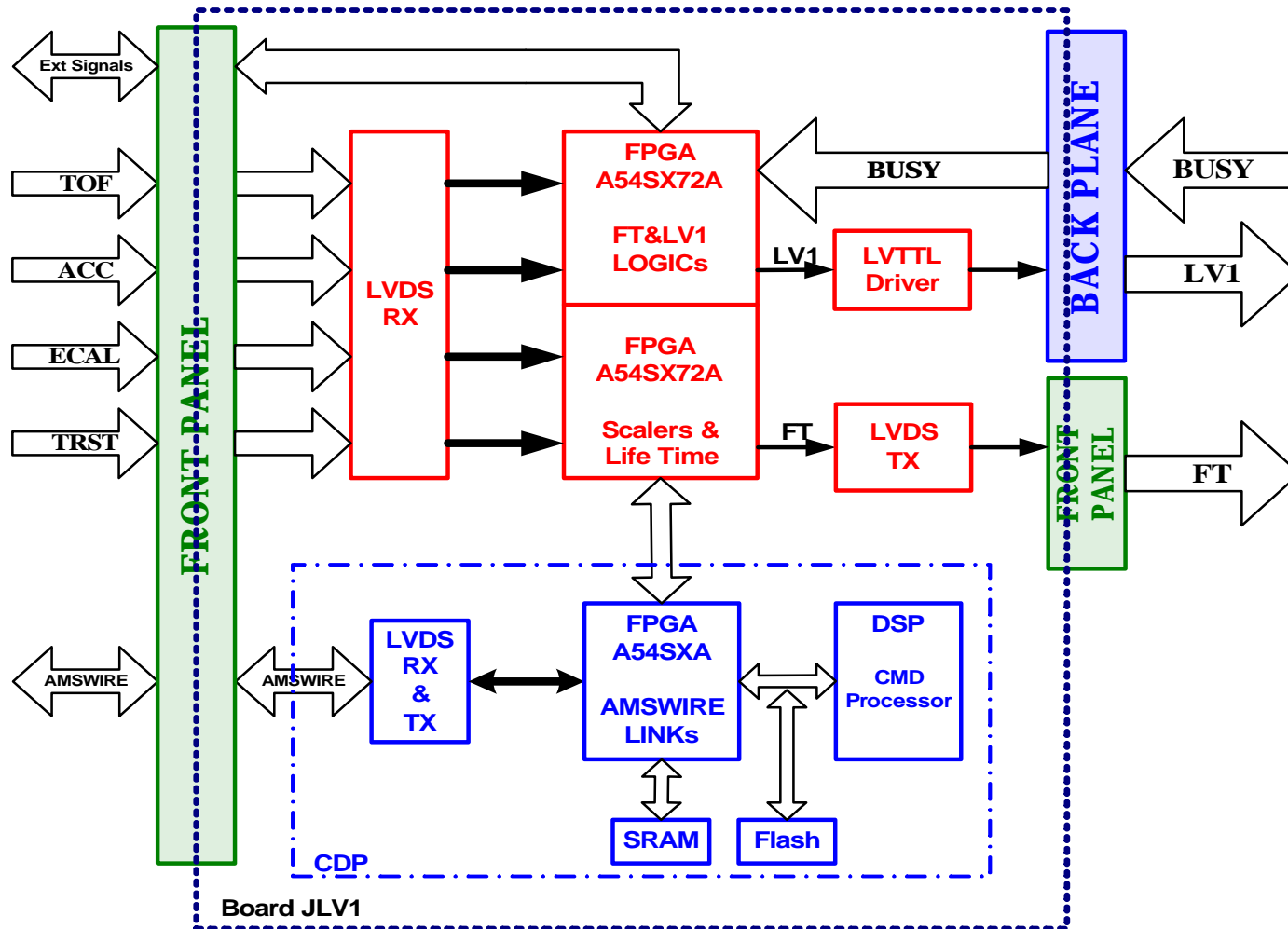
Introduction

- Requirement for AMS Trigger System
 - Provide Fast Trigger to TOF system at $\sim 150\text{ns}$ after receiving TOF signals.
 - Provide LV1 Trigger to the AMS DAQ system according to
 - ❖ Signals from TOF and ACC.
 - ❖ Signals from ECAL
 - Process requests from higher level DAQ modules via AMSWIRE links.
 - Live time measurement & Real time tap for each event.
 - Dual-Redundancy.

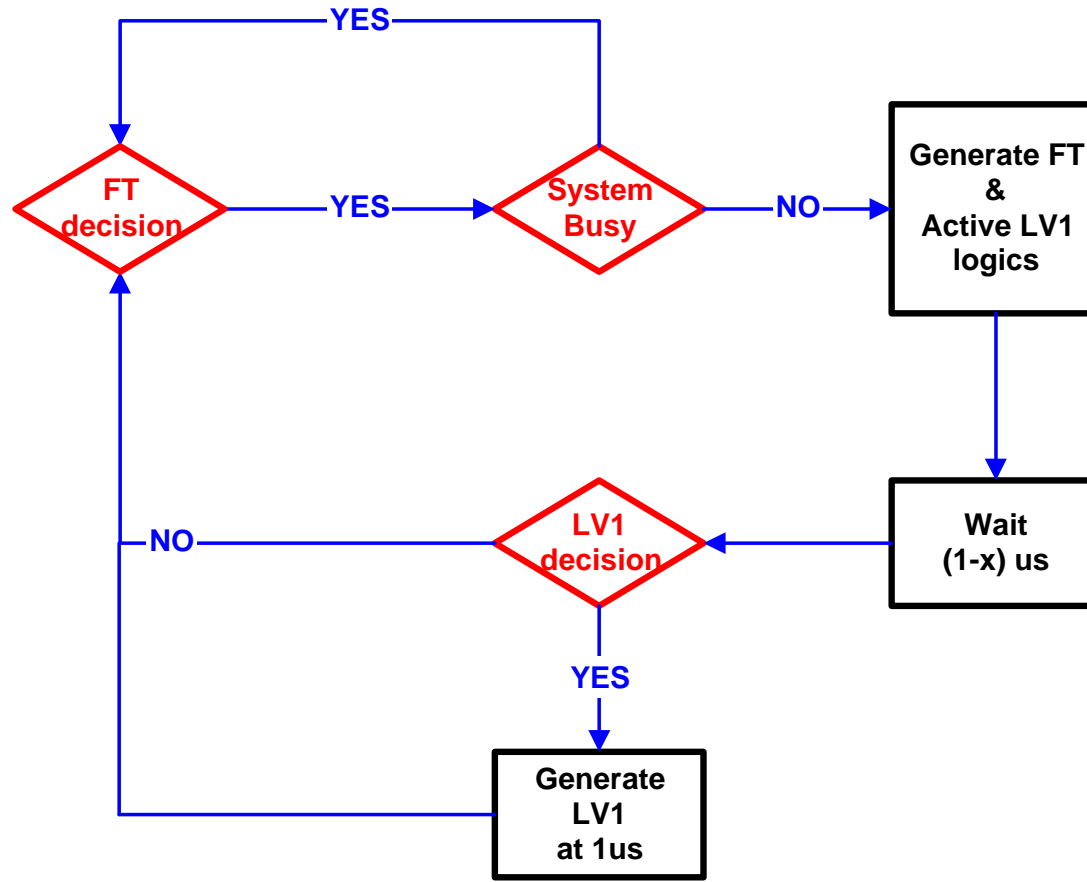
Block Diagram of Trigger System



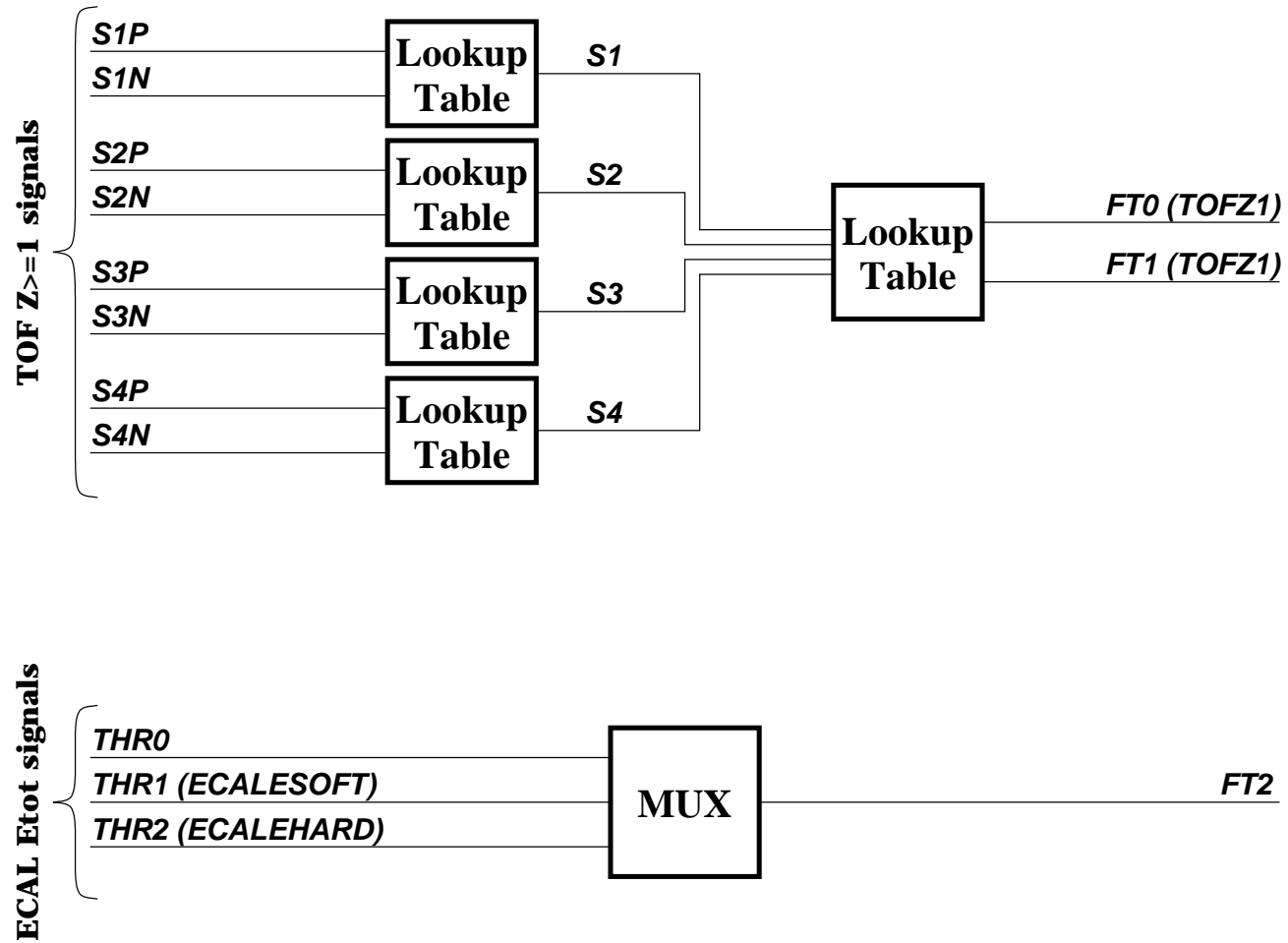
JLV1 – Block Diagram



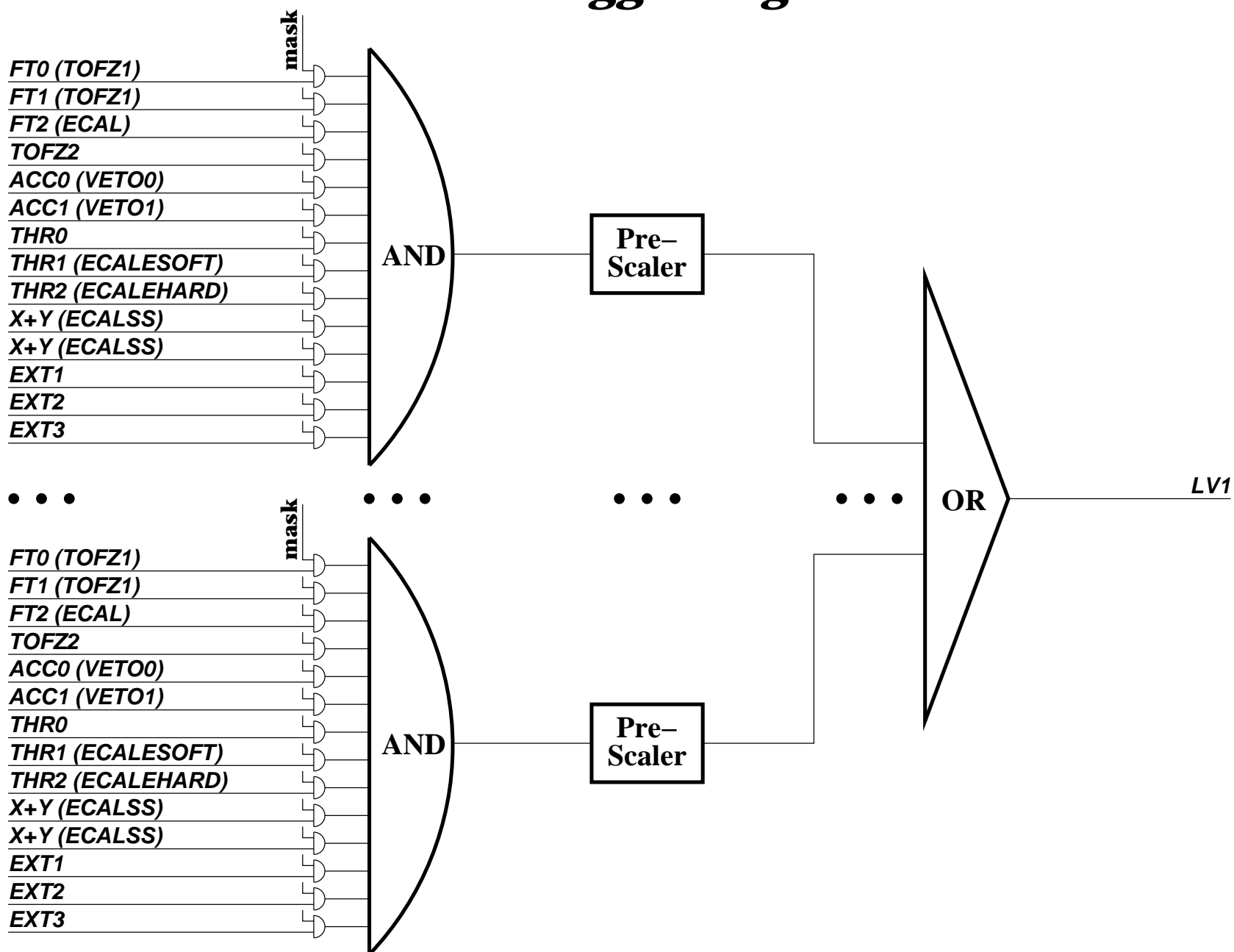
JLV1 – Trigger Logics Flow Diagram



Fast Trigger Logics



Level-1 Trigger Logics





JLV1 – System BUSY

- ❑ System Busy will prevent the Trigger distribution.
- ❑ System Busy is the OR'ing of the following busy sources :
 - ➔ Busy from JINFs and SDR2
 - ➔ External Busy from Front Panel
 - ➔ Internal Busy A
 - ❖ Set by Fast Trigger
 - ❖ Cleared by LV1 rejection or CDP
(CDP shall clear it after reading trigger info.)
 - ➔ Internal Busy B
 - ❖ Set by LV1 Trigger
 - ❖ Cleared after 1 μ s (adjustable) or by Busy from JINFs and SDR2.
 - ❖ If Busys from JINFs and SDR2 do not arrive within 1 μ s after LV1 trigger, a Busy Error signal is asserted to inform CDP.
 - ➔ Internal Busy C
 - ❖ Set by command via CDP



JLV1 – Other Functions

□ Real Time Tap :

- A time tap is given to each event when Fast Trigger is generated.
- From a 40 bit counter with 0.64 μ sec precision.

□ Scalers :

- Monitor all input signals and triggers.

□ Life Time measurement :

- A 25 bit counter is used for the life time measurement with 40ns precision in 1 sec period.



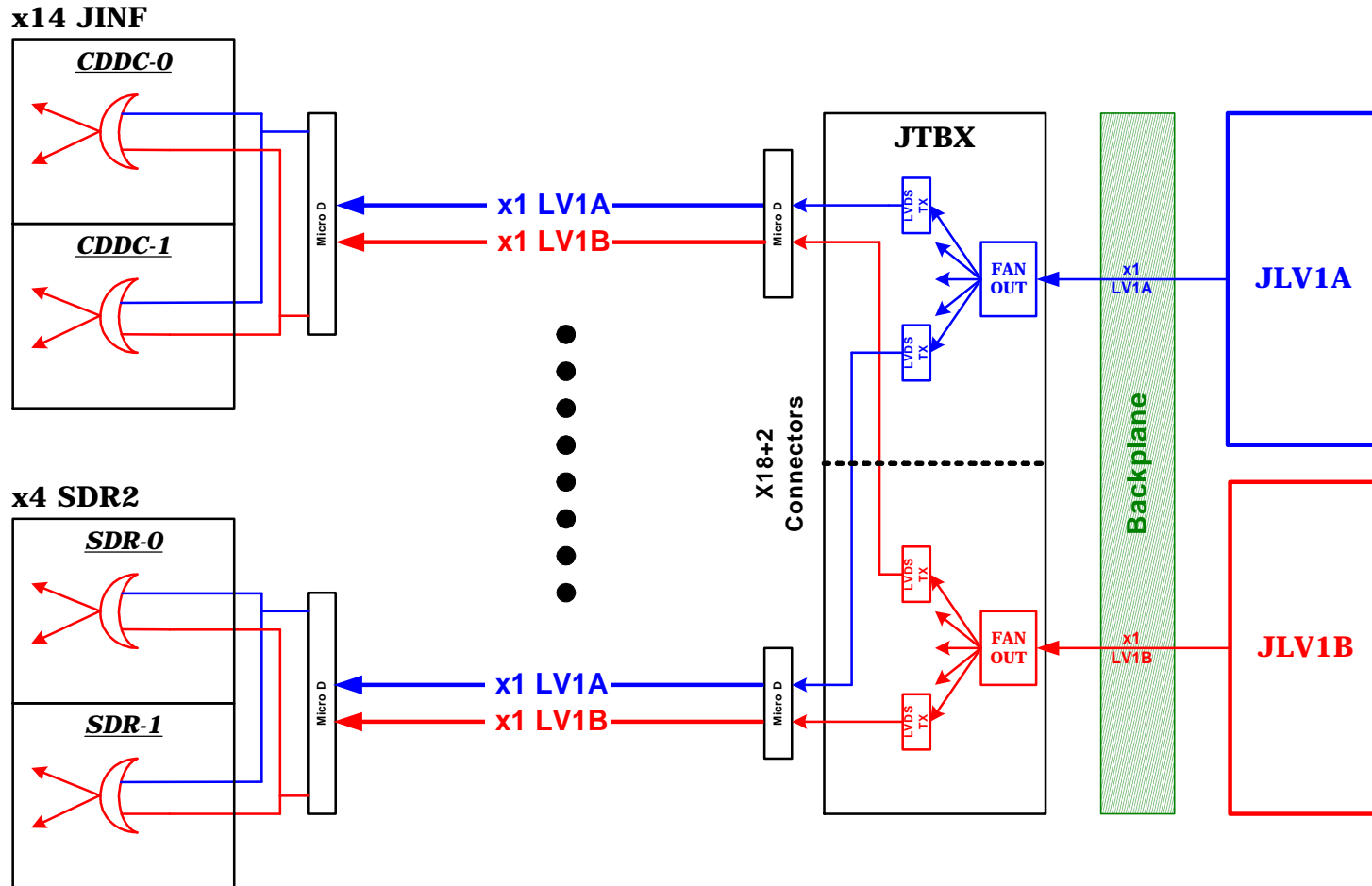
JTBX – Introduction

- JTBX is used for
 - LV1 Trigger (LV1A & LV1B) Fan-out
 - Busy signals Fan-in

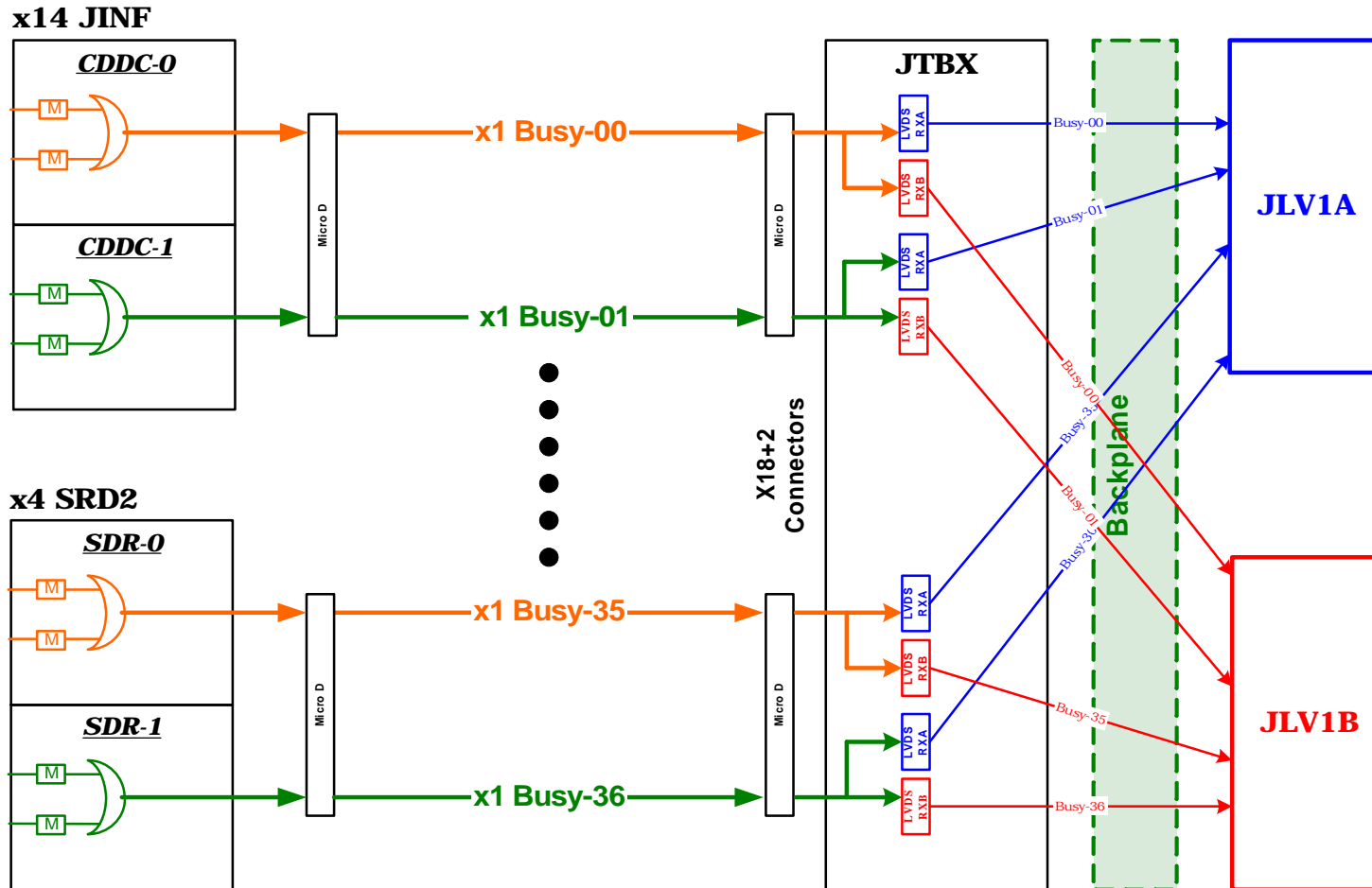
- There is no logic operation in JTBX.

- Two units, JTBXA and JTBXB
 - JTBXA is powered up together with JLV1A
 - JTBXB is powered up together with JLV1B

JTBX – LV1 Fan-Out



JTBX – Busy Fan-In





Interface Control Document

- An ICD for Trigger system is prepared:
 - ➔ Interface to TOF/ACC
 - ➔ Interface to ECAL
 - ➔ Interface to JINJ
 - ➔ Interface between JLV1 and JTBX
 - ➔ The signal type and timing is also specified.

- Require comments from TOF and ECAL group



Schedule

- EM Design based on APEX FPGA :

- Schematics and PCB layout : Done by C.H. Lin & A. Rozhkov
- PCB Production : Nov. 1st , 2002
- Board assembly : Nov. 18th , 2002

- QM Design based on A54SXA FPGA :

- Schematics : Apr. 1st , 2003