

# Flight Software Status

JSC 24 October 2007

Andrei Kounine / MIT

## xDR, JINF, JINJ software responsibilities

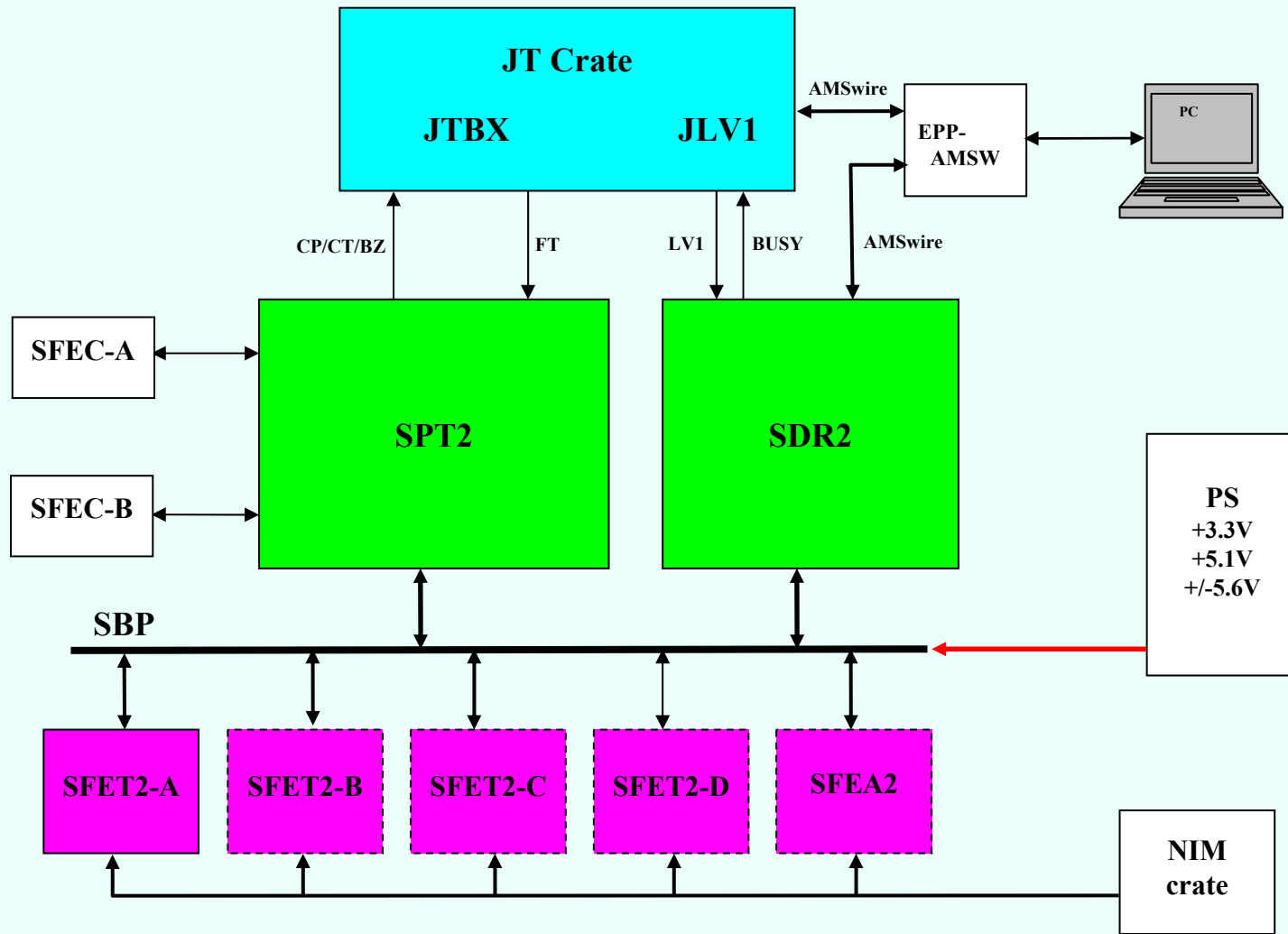
- ✓ Framework – A.Kounine
- ✓ LV1 Trigger – A.Kounine, C.H.Lin
- ✓ Tracker – D.Haas, C.Zurbach
- ✓ TRD – A.Sabellek
- ✓ RICH – G.Martinez
- ✓ ECAL – S.DiFalco
- ✓ TOF & ACC – A.Kounine

# S-crate status

# Status of S-crate development

- **S-crate comprises:**
  - Backplane (SBP);
  - 1 SDR2 board;
  - 4 SFET2 boards;
  - 1 SPT2 board (with 2 SFEC boards connected);
  - 1 SFEA2 board.
- **Test setup consist of:**
  - SBP + SDR2 boards – fully functional;
  - SPT2 + 2 SFEC boards – fully functional;
  - 2 SFET2+SFETA2 boards – FW development.
- **Software development goes along with FW development and HW verification.**

# Test Setup

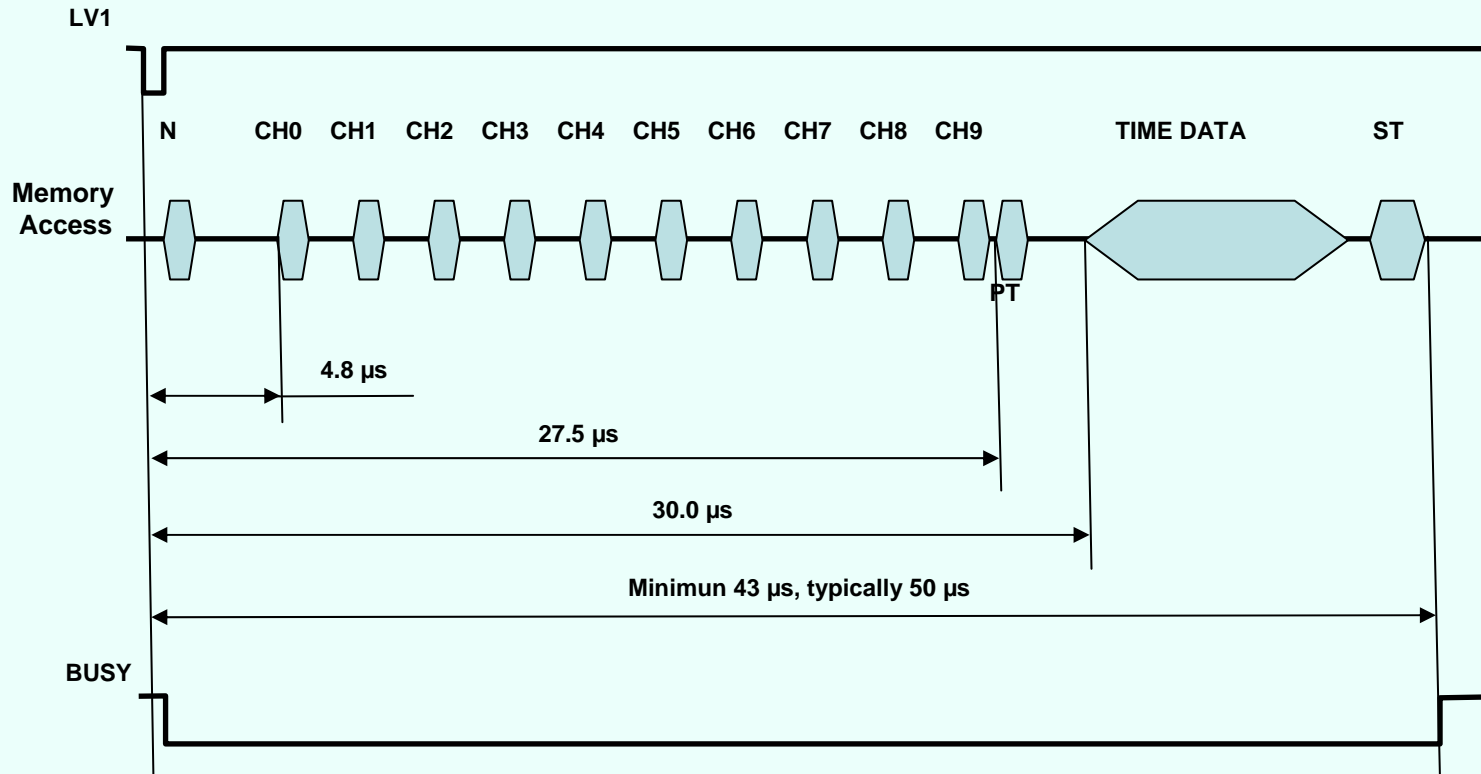


## Status of S-crate boards

- **SDR2, SPT2 boards**
  - QM boards are produced, accepted;
  - Undergo functional tests at CERN.
- **SBP board**
  - QM board is being produced;
  - EM board used for functional tests.
- **SFET2, SFEA2 boards**
  - PCB for QM are produced;
  - PCA is awaiting functional FW;
  - Development of EM boards ongoing (A.Basili).

# Data volumes and timing

# DAQ Timing - Sequencer



## DAQ Timing – Data volumes

- SDR Raw Data Format:

<b>N</b>	<b>CHARGE DATA</b>	<b>PT DATA</b>	<b>TIME DATA</b>	<b>STATUS DATA</b>	<b>ST</b>	<b>F C S</b>
<b>1w</b>	<b>90 words</b>	<b>4 words</b>	<b>variable</b>	<b>10 words</b>	<b>1w</b>	<b>1w</b>

- SDR Compressed Data Format:

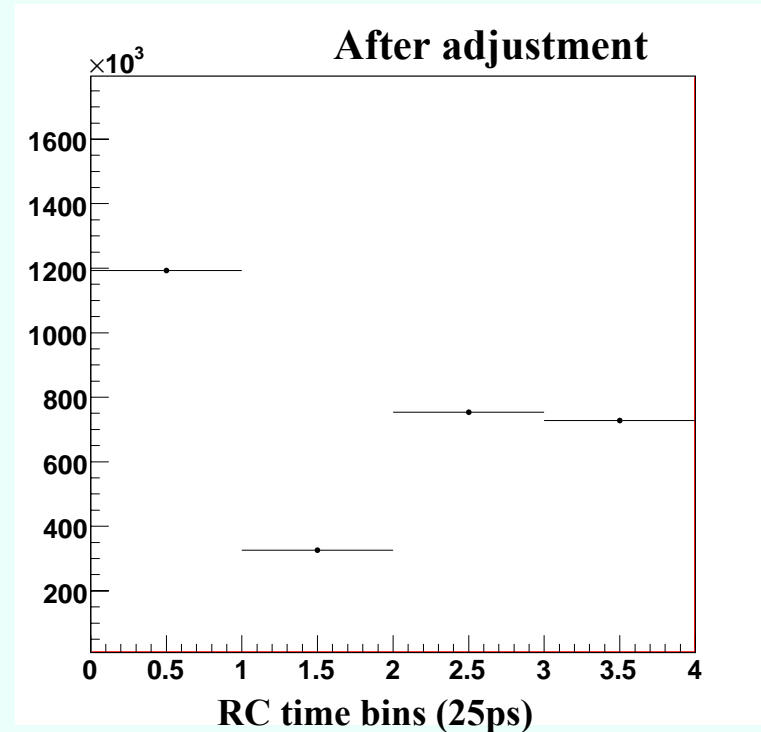
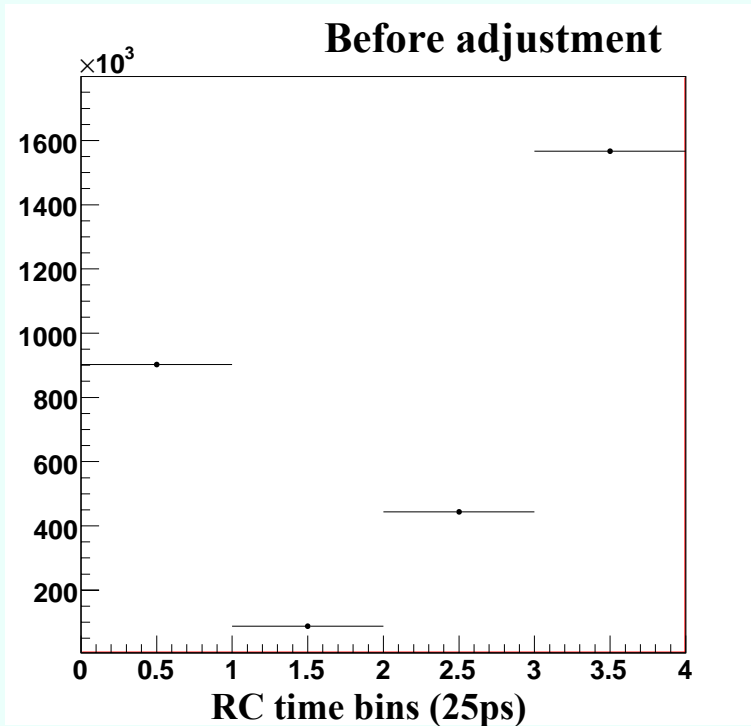
<b>N</b>	<b>PT &amp; STATUS DATA</b>	<b>CHARGE DATA</b>	<b>TIME DATA</b>	<b>ST</b>	<b>F C S</b>
<b>1w</b>	<b>7 words</b>	<b>variable</b>	<b>variable</b>	<b>1w</b>	<b>1w</b>

- **SDR Raw Data Processing**
  - Event fragment size – ~320 bytes
  - Processing time – ~60 $\mu$ s
  
- **SDR Compressed Data Processing**
  - Event fragment size – ~150 bytes
  - Processing time – ~160 $\mu$ s

# Time measurement

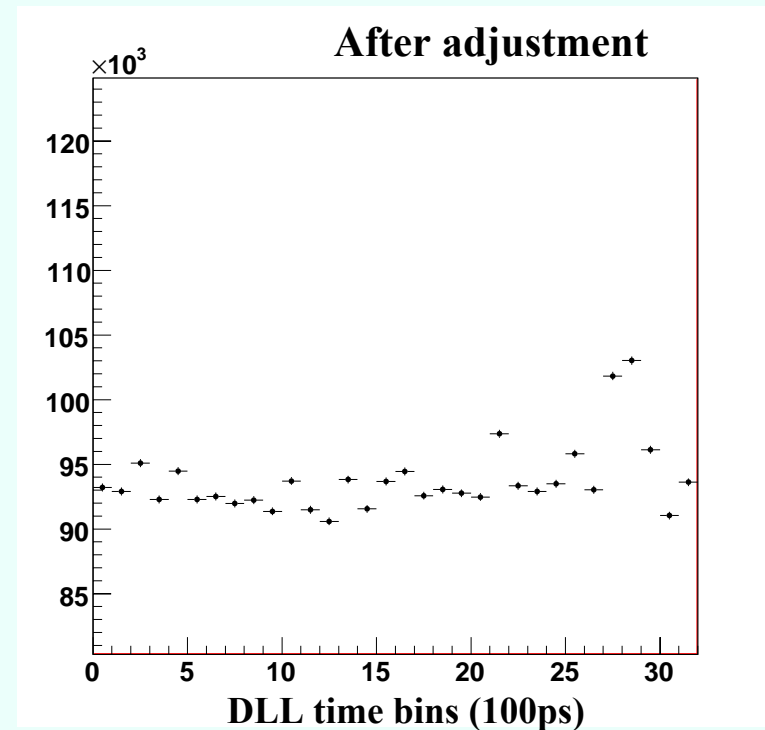
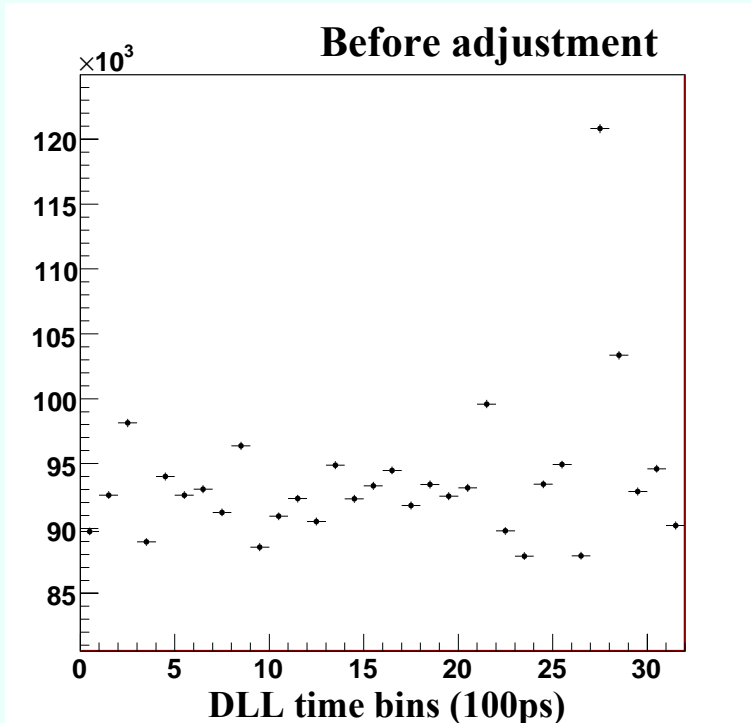
# HPTDC calibration – RC chain (4x25ps)

- 40 MHz reference clock – 25 ns
- PLL – 8 x 3.2ns
- DLL – 32 x 100ps (adjustable in HW)
- RC chain – 4 x 25ps (adjustable in HW)



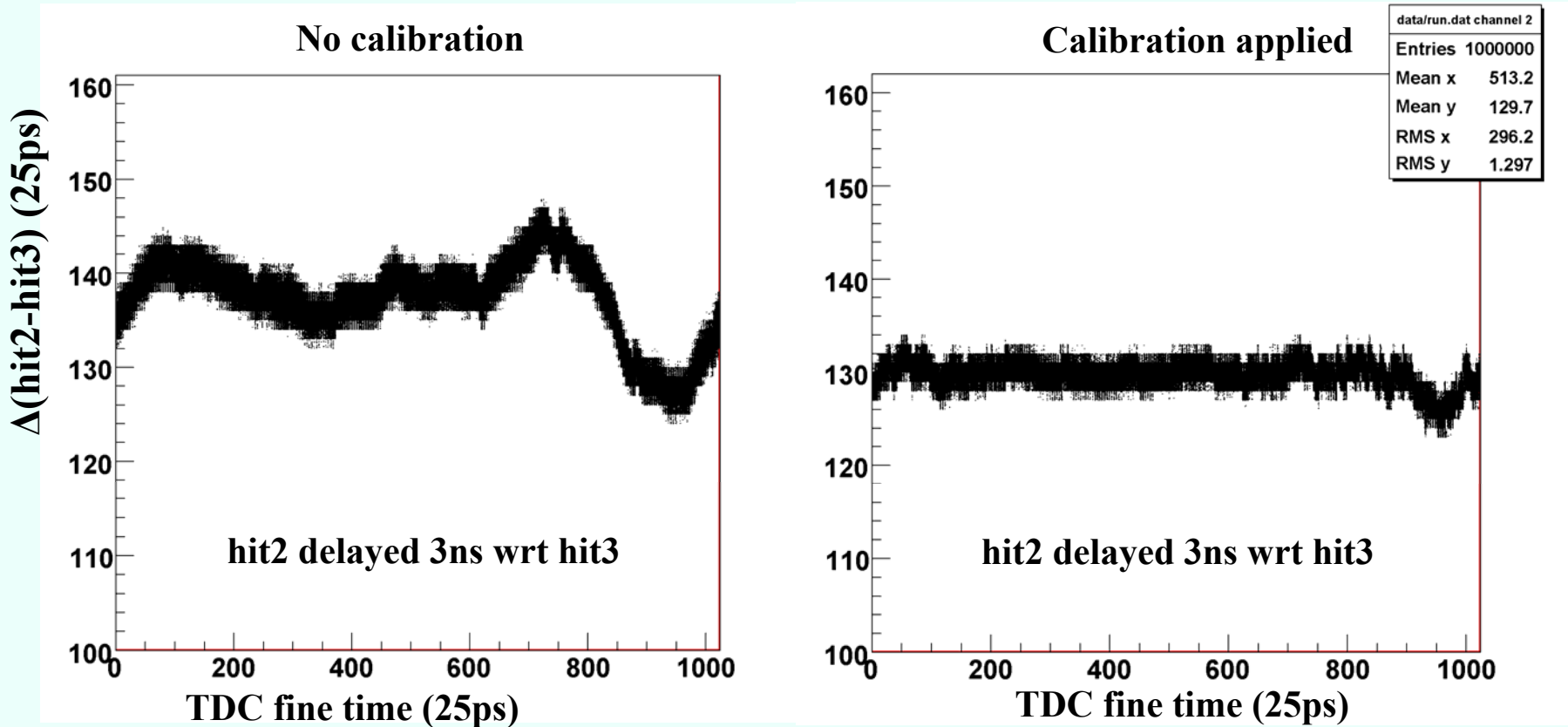
# HPTDC calibration – DLL (32x100ps)

- **32 adjustable taps (70ps overall)**
- **Loaded to HPTDC at initialisation**



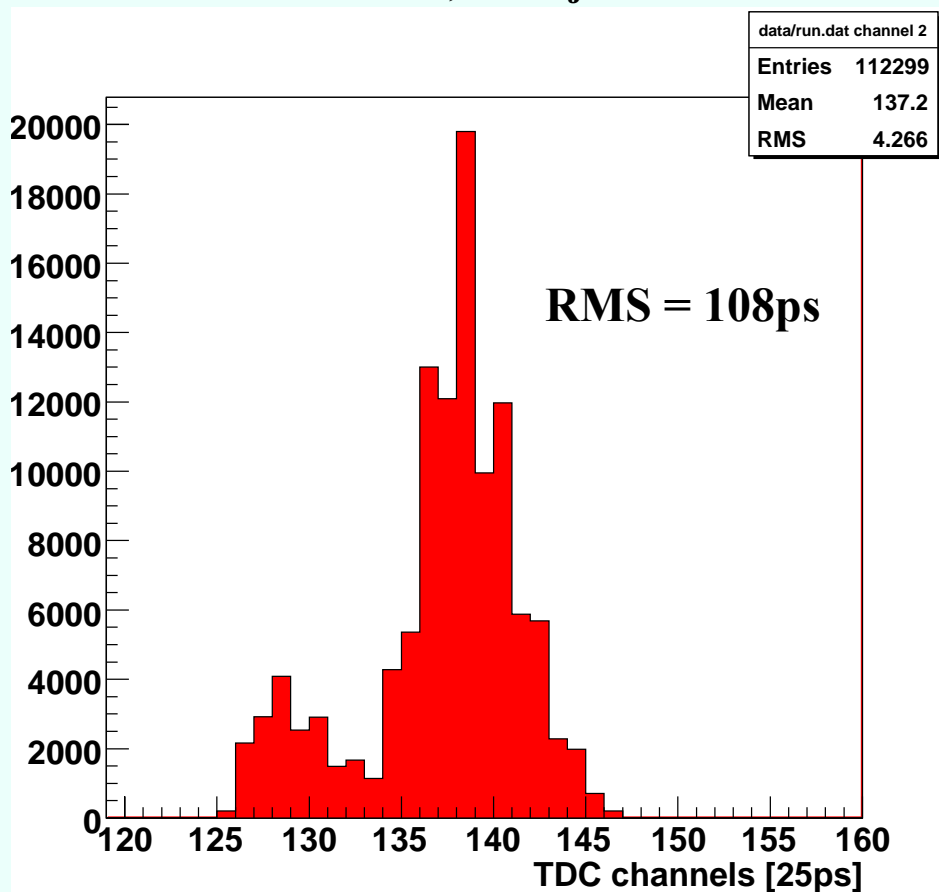
# HPTDC calibration – PLL (8x3125ps)

## Offline calibration – 8 parameters

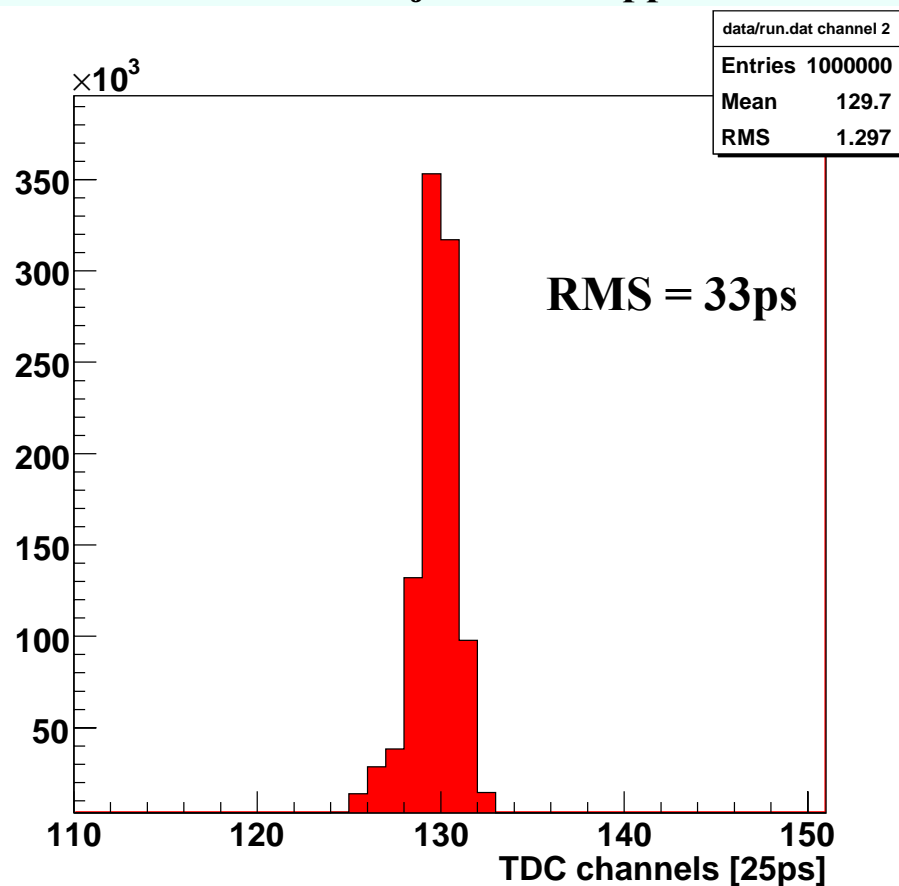


# HPTDC time measurement – same TDC

No calibration, no adjustments



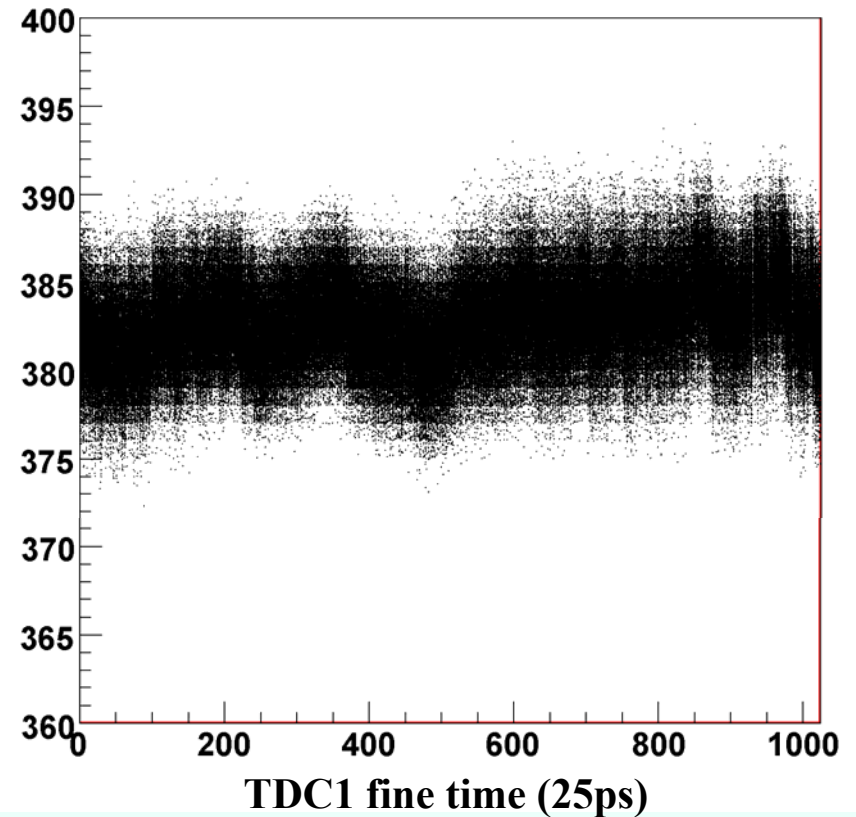
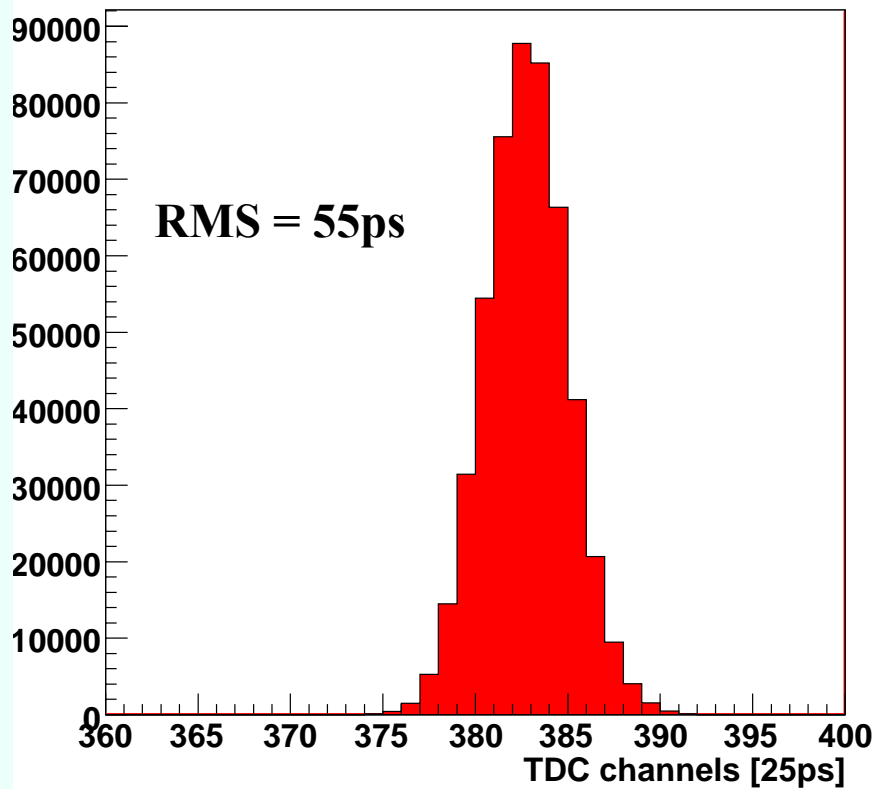
Calibration & adjustments applied



**How does it depend on the ambient conditions – still to be studied.**

# HPTDC time measurement – different S-crates

**All and same calibrations and adjustment parameters for both crates**



# S-crate schedule

## S-Crate Boards

- SBP Board
- 1 SDR2 Board
- 1 SPT2 Board
- 4 SFET2 Boards
- 1 SFEA2 Board
- EM OK, QM is being produced;
- QM, **tuning of ACTEL needed;**
- QM, no problems;
- EM tests, QM PCB produced;
- EM tests, QM PCB produced.

SFET2 and SFEA2 boards are similar.  
Aim for QM PCA “go” end of October.

# Production schedule for 2007

- 1<sup>st</sup> Nov – “GO” QM SFET2 and SFEA2 PCA;
- 15<sup>th</sup> Nov – thermal tests of QM/EM at CERN;
- 15<sup>th</sup> Nov – “GO” PCA FM SDR2, SPT2, SBP;
- 15<sup>th</sup> Nov – “GO” for PCB FM SFET2, SFEA2;
- 30<sup>th</sup> Nov – functional tests of QM SFET2/SFEA2;
- 30<sup>th</sup> Nov – rework of SDR2 QM;
- 1<sup>st</sup> Dec – “GO” for PCA FM SFET2, SFEA2;
- 15<sup>th</sup> Dec – Qualification of QM crate.